PM5384

S/UNI®-1x155

SATURN® User Network Interface (1X155) Telecom Standard Product

Datasheet

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Legal Information

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Patents

Granted

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U.S. Patent No. 5,835,602, 6,052,073, 6,150,965, 6,188,692 and 6,246,738. Canadian Patent No. 2,254,225 and 2,149,076. United Kingdom Patent No. 2,290,438. Other relevant patent grants may also exist.

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4	April 2002	- Added REFCLK Jitter Spec - Specified the correct BellCore Issue - Replace unframed with framed jitter tolerance curve. - Reliability Curve
3	April 2002	Document updated for production.
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1	September 2001	Created Document

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1 Definitions

The following table defines the abbreviations for the S/UNI-1x155.

Table 1 Acronyms

Term	Definition
AIS	Alarm Indication Signal
APS	Automatic Protection Switching
ASSP	Application Specific Standard Product
ATM	Asynchronous Transfer Mode
BER	Bit Error Rate
BIP	Byte Interleaved Parity
CBI	Common Bus Interface
CMOS	Complementary Metal Oxide Semiconductor
CRC	Cyclic Redundancy Check
CRSI	CRU and Serial-In Parallel-Out
CRU	Clock Recovery Unit
CSPI	CSU and Parallel-In Serial-Out
CSU	Clock Synthesis Unit
DCC	Data Communication Channel
DRU	Data Recovery Unit
ECL	Emitter Controlled Logic
ERDI	Enhanced Remote Defect Indication
ESD	Electrostatic Discharge
FCS	Frame Check Sequence
FEBE	Far-End Block Error also referred to as REI
FIFO	First-In First-Out
GFC	Generic Flow Control
HCS	Header Check Sequence
HDLC	High-level Data Link Layer
LAN	Local Area Network
LCD	Loss of Cell Delineation
LOF	Loss of Frame
LOH	Line Overhead
LOP	Loss of Pointer
LOS	Loss of Signal
LOT	Loss of Transition
LAIS	Line AIS also referred to as AIS-L
LRDI	Line RDI also referred to as RDI-L
NC	No Connect, indicates an unused pin
NDF	New Data Flag

Term	Definition
NNI	Network-Network Interface
ODL	Optical Data Link
OOF	Out of Frame
PECL	Pseudo-ECL
PLL	Phase-Locked Loop
POS	Packet Over SONET
PPP	Point-to-Point Protocol
PSL	Path Signal Label
PSLM	Path Signal Label Mismatch
RAPS	Receive APS Interface
RAOP	Receive APS Overhead Processor
RASE	Receive APS, Synchronization Extractor and Bit Error Monitor
RDI	Remote Defect Indication
RLOP	Receive Line Overhead Processor
RPOP	Receive Path Overhead Processor
RSOP	Receive Section Overhead Processor
RXCP	Receive ATM Cell Processor
RXFP	Receive POS Frame Processor
SBGA	Super Ball Grid Array
SD	Signal Degrade (alarm), Signal Detect (pin)
SDH	Synchronous Digital Hierarchy
SF	Signal Fail
SOH	Section Overhead
SONET	Synchronous Optical Network
SPE	Synchronous Payload Envelope
SPTB	SONET/SDH Path Trace Buffer
SSTB	SONET/SDH Section Trace Buffer
TAPS	Transmit APS Interface
TIM	Trace Identifier Mismatch
TIU	Trace Identifier Unstable
TAOP	Transmit APS Overhead Processor
TLOP	Transmit Line Overhead Processor
TOH	Transport Overhead
TPOP	Transmit Path Overhead Processor
TSOP	Transmit Section Overhead Processor
TXCP	Transmit ATM Cell Processor
TXFP	Transmit POS Frame Processor
UI	Unit Interval
UNI	User-Network Interface
VCI	Virtual Connection Indicator

Term	Definition
VCXO	Voltage Controlled Oscillator
VPI	Virtual Path Indicator
WAN	Wide Area Network
XOR	Exclusive OR logic operator

2 Features

2.1 General

- Single chip ATM and Packet over SONET/SDH Physical Layer Device operating at 155.52 Mbit/s.
- Implements the ATM Forum User Network Interface Specification and the ATM physical layer for Broadband ISDN according to ITU Recommendation I.432.
- Implements the Point-to-Point Protocol (PPP) over SONET/SDH specification according to RFC 2615 and RFC 1662.
- Processes duplex bit-serial 155.52 Mbit/s STS-3c/STM-1 data streams with on-chip clock and data recovery and clock synthesis.
- Complies with Bellcore GR-253-CORE (2000 Issue) jitter tolerance, jitter transfer (1995 Issue) and intrinsic jitter criteria.
- Provides control circuitry required to comply with Bellcore GR-253-CORE WAN clocking requirements related to wander transfer, holdover and long term stability when using an external VCXO.
- Provides UTOPIA Level2™ 8-bit wide System Interface (clocked up to 52 MHz) with parity support for ATM applications.
- Provides UTOPIA Level 2™ 16-bit wide System Interface (clocked up to 52 MHz) with parity support for ATM applications.
- Provides SATURN POS-PHY Level 2™ 16-bit System Interface (clocked up to 52 MHz) for Packet over SONET/SDH (POS) applications. This system interface is similar to UTOPIA Level 2, but adapted to packet transfer.
- Provides support functions for 1+1 APS operation.
- Provides a standard 5 signal IEEE 1149.1 JTAG test port for boundary scan board test purposes.
- Provides a generic 8-bit microprocessor bus interface for configuration, control, and status monitoring.
- Low power 2.5/3.3 volt CMOS with 5 volt TTL compatible digital inputs outputs. PECL inputs and outputs are 3.3 volt and 5 volt compatible.
- Industrial temperature range (-40°C to +85°C).
- 15x15mm 196 pin stPBGA package with 1mm ball pitch.

2.2 The SONET Receiver

- Provides a serial interface at 155.52 Mbit/s with clock and data recovery.
- Frames to and de-scrambles the received STS-3c/STM-1 streams.
- Interprets the received payload pointers (H1, H2) and extracts the STS-3c/STM-1 synchronous payload envelopes and path overheads.

- Extracts the data communication channels (D1-D3, D4-D12) and serializes them at 192 kbit/s (D1-D3) and 576 kbit/s (D4-D12) for optional external processing.
- Extracts all transport overhead bytes and serializes them at 5.184 Mbit/s for optional external processing.
- Extracts all path overhead bytes and serializes them at 576 kbit/s for optional external processing.
- Filters and captures the automatic protection switch channel (APS) bytes in readable registers and detects APS byte failure.
- Captures and de-bounces each synchronization status (S1) nibble in a readable register.
- Detects signal degrade (SD) and signal fail (SF) threshold crossing alarms based on received B2 errors.
- Extracts the 16-byte or 64-byte section trace (J0/Z0) sequences and the 16-byte or 64-byte path trace (J1) sequences into internal register banks.
- Detects loss of signal (LOS), out of frame (OOF), loss of frame (LOF), line alarm indication signal (AIS-L), line remote defect indication (RDI-L), loss of pointer (LOP), path alarm indication signal (AIS-P), path remote defect indication (RDI-P), and path extended remote defect indicator (extended RDI-P).
- Counts received section BIP-8 (B1) errors, received line BIP-24 (B2) errors, line remote error indicates (REI-L), received path BIP-8 (B3) errors and path remote error indications (REI-P) for performance monitoring purposes.

2.3 The Receive ATM Processor

- Extracts ATM cells from the received STS-3c/STM-1 payload using ATM cell delineation.
- Provides ATM cell payload de-scrambling.
- Performs header check sequence (HCS) error detection and correction, and idle/unassigned cell filtering.
- Detects out of cell Delineation (OCD) and loss of cell delineation (LCD) alarms.
- Counts number of received cells, idle cells, errored cells and dropped cells.
- Provides a UTOPIA Level 2 compliant 8-bit wide datapath interface (clocked up to 52 MHz) with parity support to read extracted cells from an internal four-cell FIFO buffer.
- Provides a UTOPIA Level 2 compliant 16-bit wide datapath interface (clocked up to 52 MHz) with parity support to read extracted cells from an internal four-cell FIFO buffer.

2.4 The Receive POS Processor

- Supports packet based link layer protocols using byte synchronous HDLC framing like PPP, HDLC and Frame Relay.
- Performs self-synchronous POS data de-scrambling on the received STS-3c/STM-1 payload using the $x^{43}+1$ polynomial.
- Performs flag sequence detection and terminates the received POS frames.

- Performs frame check sequence (FCS) validation for CRC-16.ISO-3309 and CRC-32 polynomials.
- Performs control escape de-stuffing of the HDLC stream.
- Detects for packet abort sequence.
- Checks for minimum and maximum packet lengths. Optionally deletes short packets and marks those exceeding the maximum length as errored.
- Provides a SATURN POS-PHY Level 2 compliant 16-bit datapath interface (clocked up to 52 MHz) with parity support to read packet data from an internal 256 byte FIFO buffer.

2.5 The SONET Transmitter

- Synthesizes the 155.52 MHz transmit clock from a 19.44 MHz reference.
- Provides a differential PECL bit-serial interface at 155.52 Mbit/s.
- Inserts register programmable path signal label (C2).
- Generates the transmit payload pointers (H1, H2) and inserts path overhead.
- Optionally inserts the 16-byte or 64-byte section trace (J0/Z0) sequence and the 16-byte or 64-byte path trace (J1) sequence from internal register banks.
- Optionally inserts externally generated data communication channels (D1-D3, D4-D12) via a 192 kbit/s (D1-D3) serial stream and a 576 kbit/s (D4-D12) serial stream.
- Optionally inserts externally generated path overhead bytes received via a 576 kbit/s serial interface.
- Optionally inserts externally generated transport overhead bytes received via a 5.184 Mbit/s serial interface
- Scrambles the transmitted STS-3c/STM-1 stream and inserts the framing bytes (A1, A2).
- Optionally inserts register programmable APS bytes.
- Provides support allowing two devices to implement 1+1 APS.
- Inserts path BIP-8 codes (B3), path remote error indications (REI-P), line BIP-24 codes (B2), line remote error indications (REI-L), and section BIP-8 codes (B1) to allow performance monitoring at the far end.
- Allows forced insertion of all-zeros data (after scrambling) and the corruption of the section, line, or path BIP-8 codes for diagnostic purposes.
- Inserts ATM cells or POS frames into the transmitted STS-3c/STM-1 payload.

2.6 The Transmit ATM Processor

- Provides idle/unassigned cell insertion.
- Provides HCS generation/insertion, and ATM cell payload scrambling.
- Counts number of transmitted and idle cells.

- Provides a UTOPIA Level 2 compliant 8-bit wide datapath interface (clocked up to 52 MHz) with parity support for writing cells into an interface four-cell FIFO.
- Provides a UTOPIA Level 2 compliant 16-bit wide datapath interface (clocked up to 52 MHz) with parity support for writing cells into an internal four-cell FIFO.

2.7 The Transmit POS Processor

- Supports any packet based link layer protocol using byte synchronous HDLC framing like PPP, HDLC and Frame Relay.
- Performs self-synchronous POS data scrambling using the $x^{43}+1$ polynomial.
- Encapsulates packets within a POS frame.
- Performs flag sequence insertion.
- Performs byte stuffing for transparency processing.
- Performs frame check sequence generation using the CRC-16.ISO-3309 and CRC-32 polynomials.
- Aborts packets under the direction of the host or when the FIFO underflows.
- Provides a SATURN POS-PHY Level 2 compliant 16-bit wide datapath (clocked up to 52 MHz) with parity support to an internal 256 byte FIFO buffer.

2.8 APS Support

- Allows the channel to be bridged on the transmit direction at the SONET/SDH path level with another S/UNI-1x155 device, support 1+1 APS interfaces.
- With two S/UNI-1x155 devices, supports one 1+1 APS interface.
- Provides one transmit differential PECL bit-serial interfaces at 155.52 Mbit/s to source transmit channel (bridge) with a second S/UNI-1x155 device at the SONET/SDH path level.
- Provides one receive differential PECL bit-serial interface at 155.52 Mbit/s to source transmit channel (bridge) with a second S/UNI-1x155 device at the SONET/SDH path level.
- Provides performance monitoring of bit errors across the receive stream.

3 Applications

- WAN and Edge ATM switches.
- LAN switches and hubs.
- Packet switches and hubs.
- Routers and Layer 3 Switches
- Network Interface Cards and Uplinks

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- PMC-1971147, *Saturn Compliant Interface for Packet over SONET Physical Layer and Link Layer Devices, Level 2*, January 1998.
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5 Application Examples

The PM5384 S/UNI-1x155 is applicable to equipment implementing Asynchronous Transfer Mode (ATM) User-Network Interfaces (UNI), ATM Network-Network Interfaces (NNI), as well as Packet over SONET/SDH (POS) interfaces. The POS interface can support several packet-based protocols, including the Point-to-Point Protocol (PPP).

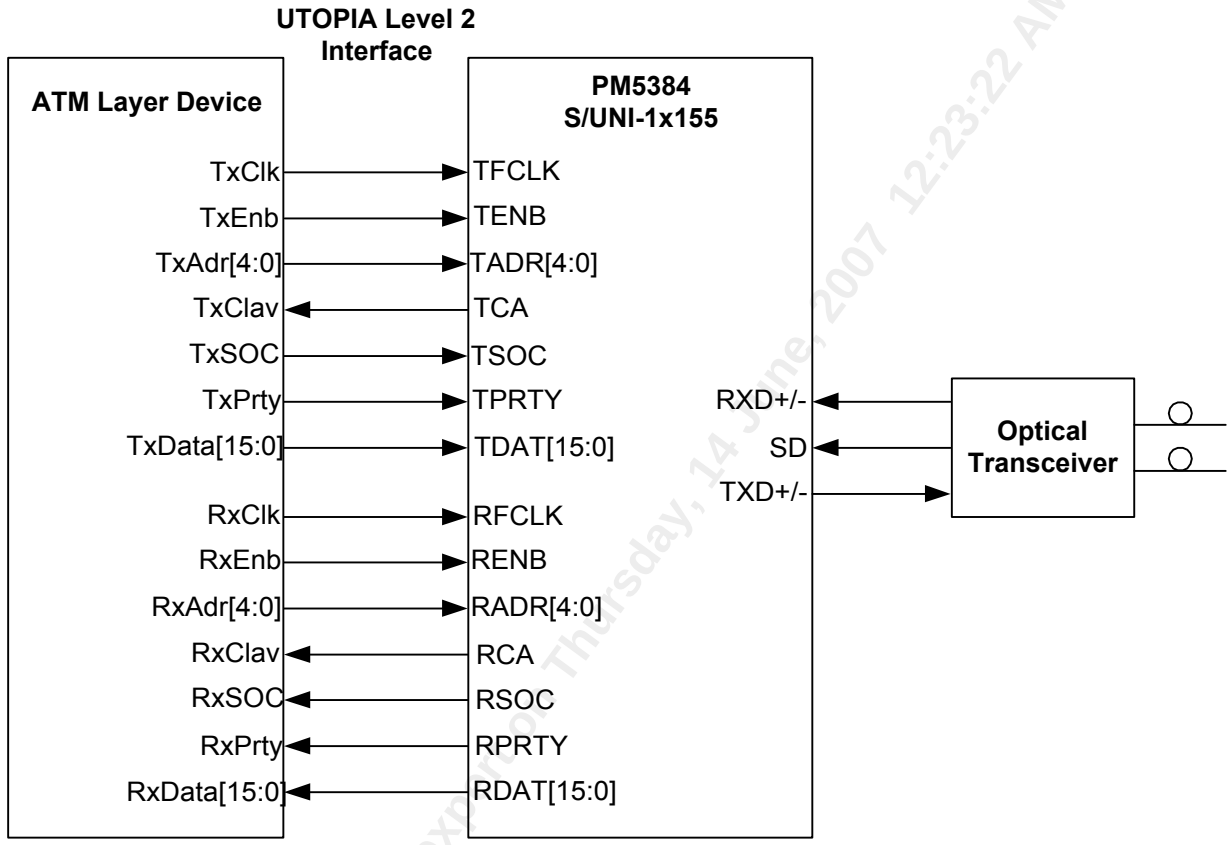
The S/UNI-1x155 may find application at either end of switch-to-switch links or switch-to-terminal links, both in public network (WAN) and private network (LAN) situations. The S/UNI-1x155 provides a comprehensive feature set. The S/UNI-1x155 performs the mapping of either ATM cells or POS frames into the SONET/SDH STS-3c/STM-1 synchronous payload envelope (SPE) and processes applicable SONET/SDH section, line and path overheads for one channel.

In a typical STS-3c/STM-1 ATM application, the S/UNI-1x155 performs clock and data recovery in the receive direction and clock synthesis in the transmit direction of the line interface.

On the system side, the S/UNI-1x155 interfaces directly with ATM layer processors and switching or adaptation functions using an UTOPIA Level 2 compliant 16-bit or 8-bit (clocked up to 52 MHz) synchronous FIFO style interface.

An application with a UTOPIA Level 2 system side is shown in Figure 1. The initial configuration and ongoing control and monitoring of the S/UNI-1x155 are normally provided via a generic microprocessor interface.

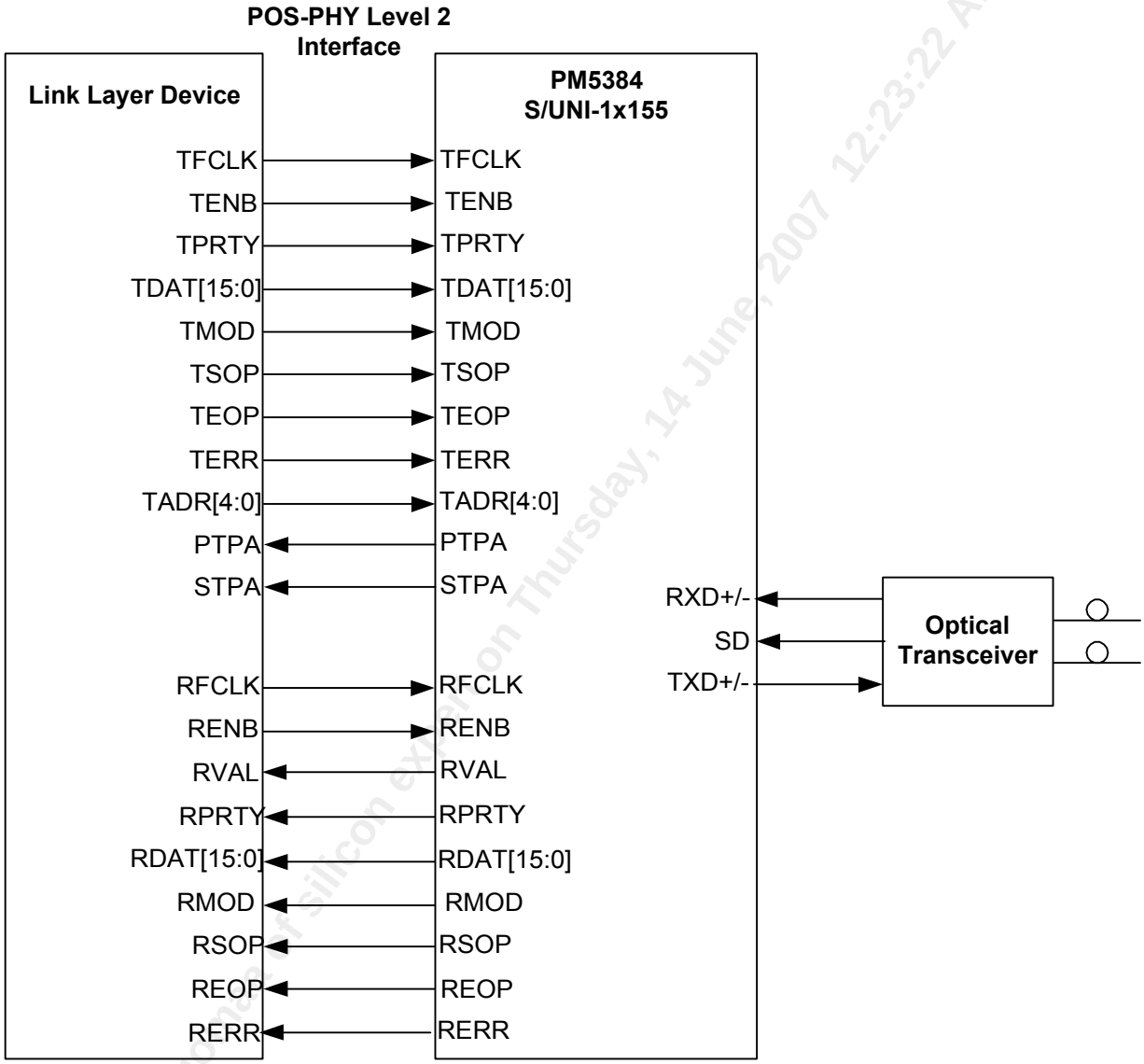
Figure 1 Typical STS-3c/STM-1 ATM Switch Port Application



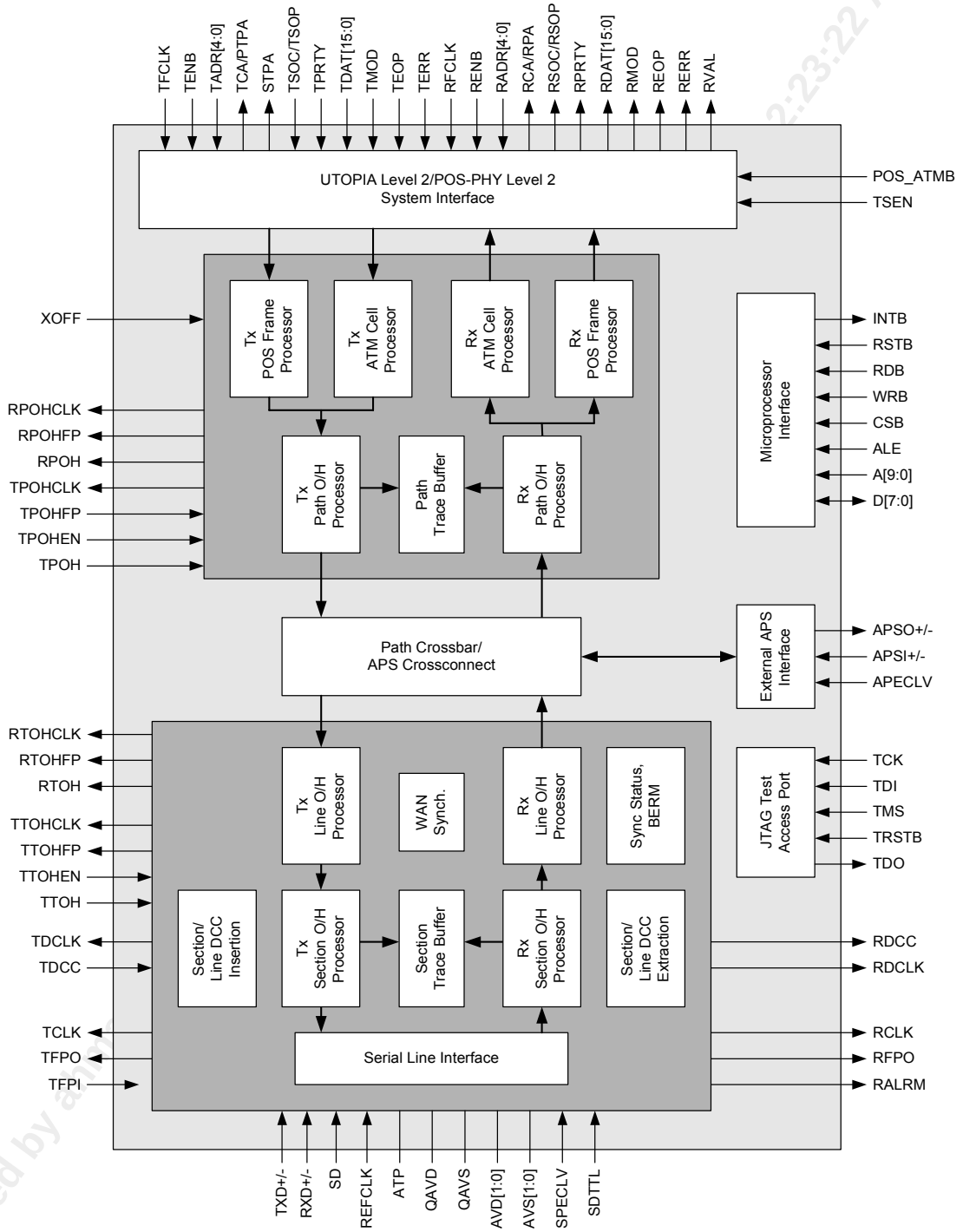
In a typical Packet over SONET/SDH application (i.e. using the PPP protocol) the S/UNI-1x155 performs clock and data recovery in the receive direction and clock synthesis in the transmit direction of the line interface. On the system side, the S/UNI-1x155 interfaces directly with a data link layer processor using a SATURN POS-PHY Level 2 16-bit (clocked up to 52 MHz) synchronous FIFO interface over which packets are transferred.

An application with a POS-PHY Level 2 interface is shown in Figure 2. The initial configuration and ongoing control and monitoring of the S/UNI-1x155 are normally provided via a generic microprocessor interface.

Figure 2 Typical STS-3c/STM-1 Packet over SONET/SDH Application



6 Block Diagram



7 Description

The PM5384 S/UNI-1x155 SATURN User Network Interface is a monolithic integrated circuit that implements SONET/SDH processing, ATM mapping and Packet over SONET/SDH mapping functions at the STS-3c/STM-1 155.52 Mbit/s rate.

The S/UNI-1x155 receives SONET/SDH streams using a bit serial interface, recovers the clock and data and processes section, line, and path overhead. The S/UNI-1x155 performs framing (A1, A2), de-scrambling, detects alarm conditions, and monitors section, line, and path bit interleaved parity (B1, B2, B3), accumulating error counts at each level for performance monitoring purposes. Line and path remote error indications (M1, G1) are also accumulated. The S/UNI-1x155 interprets the received payload pointers (H1, H2) and extracts the synchronous payload envelope which carries the received ATM cell or POS frame payload.

When used to implement an ATM UNI or NNI, the S/UNI-1x155 frames to the ATM payload using cell delineation. Idle/unassigned cells may be optionally dropped. Cells are also dropped upon detection of an uncorrectable header check sequence error. The ATM cell payloads are descrambled and are written to a 64 cell FIFO buffer. The received cells are read from the FIFO using a 16 bit/8 bit wide UTOPIA Level 2 (clocked up to 52 MHz) or a 16 bit wide POS-PHY Level 2 (clocked up to 52 MHz) system side interface. Counts of received ATM cell headers that are erred and uncorrectable and those that are erred and correctable are accumulated independently for performance monitoring purposes.

When used to implement packet transmission over a SONET/SDH link, the S/UNI-1x155 extracts Packet over SONET/SDH (POS) frames from the SONET/SDH synchronous payload envelope. Frames are verified for correct construction and size. The control escape characters are removed. The frame check sequence is optionally verified for correctness and the extracted packets are placed in a 256 byte receive FIFO. The received packets are read from the FIFO through a 16 bit POS-PHY Level 2 (clocked up to 52 MHz) system side interface. Valid and FCS errored packet counts are provided for performance monitoring. The S/UNI-1x155 Packet over SONET/SDH implementation is flexible enough to support several link layer protocols, including HDLC, PPP and Frame Relay.

The S/UNI-1x155 synthesizes the transmit clock from a 19.44 MHz frequency reference and performs framing pattern insertion (A1, A2), scrambling, alarm signal insertion, and creates section, line, and path bit interleaved parity codes (B1, B2, B3) as required to allow performance monitoring at the far end. Line and path remote error indications (M1, G1) are also inserted. The S/UNI-1x155 generates the payload pointer (H1, H2) and inserts the synchronous payload envelope that carries the ATM cell or POS frame payload. .

When used to implement an ATM UNI or NNI, ATM cells are written to an internal 64 cell FIFO using a 16 bit/8 bit wide UTOPIA Level 2 (clocked up to 52 MHz) or a 16 bit width POS-PHY Level 2 (clocked up to 52 MHz) system side interface. Idle/unassigned cells are automatically inserted when the internal FIFO contains less than one complete cell. The S/UNI-1x155 provides generation of the header check sequence and scrambles the payload of the ATM cells. Each of these transmit ATM cell processing functions can be enabled or bypassed.

When used to implement a Packet over SONET/SDH link, the S/UNI-1x155 inserts POS frames into the SONET/SDH synchronous payload envelope. Packets to be transmitted are written into a 256 byte FIFO through a 16 bit SATURN POS-PHY Level 2 (clocked up to 52 MHz) system side interface. POS frames are built by inserting the flags, control escape characters and the FCS fields. Either the CRC-16.ISO-3309 or CRC-32 can be computed and added to the frame. Several counters are provided for performance monitoring.

No line rate clocks are required directly by the S/UNI-1x155 as it synthesizes the transmit clock and recovers the receive clock using a 19.44 MHz reference clock. The S/UNI-1x155 also provides WAN Synchronization controllers that can be used to control an external VCXO in order to fully meet Bellcore GR-253-CORE jitter, wander, holdover and stability requirements.

The S/UNI-1x155 also contains internal crossbar logic that allows the transmit streams to be bridged between devices at the SONET/SDH path level. Two S/UNI-1x155 devices may exchange SONET/SDH path streams using the 155.52 MHz serial APS link. Error detection and performance monitoring features are provided for the serial APS link.

The S/UNI-1x155 is configured, controlled and monitored via a generic 8-bit microprocessor bus interface. The S/UNI-1x155 also provides a standard 5 signal IEEE 1149.1 JTAG test port for boundary scan board test purposes.

The S/UNI-1x155 is implemented in low power, 2.5/3.3 volt CMOS technology. It has 5.0 volt TTL compatible digital inputs and outputs. High speed inputs and outputs support 3.3 volt and 5.0 volt compatible pseudo-ECL (PECL). The S/UNI-1x155 is packaged in a 196 pin stPBGA package.

8 Pin Diagram

The S/UNI-1x155 is available in a 196-pin stPBGA package having a body size of 15 mm by 15 mm and a ball pitch of 1 mm.

	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	TDAT[3]	TDAT[4]	TDAT[5]	TDAT[7]	TDAT[10]	TDAT[12]	D[0]	D[3]	A[3]	A[8]	ALE	RDB	CSB	VDDQ	A
B	TDAT[1]	TDAT[2]	TDAT[6]	TDAT[8]	VSSO	TDAT[13]	VSSI	D[4]	VSSO	A[7]	VSSO	RSTB	WRB	VSSQ	B
C	TDAT[0]	TENB	TERR	TDAT[9]	VDDO	TDAT[14]	VDDI	D[5]	VDDO	A[6]	VDDO	INTB	VSSO	VDDO	C
D	TEOP	VSSO	VDDO	TMOD	TDAT[11]	TDAT[15]	D[1]	D[6]	A[2]	A[5]	A[9]	VSSO	APSO-	APSO+	D
E	TSOC_ TSOP	TADR[0]	TADR[1]	STPA	TCA_ PTPA	TPRTY	D[2]	D[7]	A[1]	A[4]	SDTTL	VDDO	VSSO	VDDO	E
F	TFCLK	VSSO	VDDO	TADR[2]	TADR[3]	TADR[4]	NC	TSEN	A[0]	VDDI	VSSO	VDDO	TXD-	TXD+	F
G	RFCLK	VSSI	VDDI	RADR[0]	RADR[1]	XOFF	NC	NC	NC	VSSI	VSSO	VDDO	VSSO	VDDO	G
H	RADR[2]	VSSO	VDDO	RADR[3]	RADR[4]	NC	NC	NC	ATP	AVD[1]	AVS[1]	SD	RXD-	RXD+	H
J	RENB	RERR	REOP	RPRTY	RSOC_ RSOP	RDAT[2]	POS_ ATMB	NC	SPECLV	APECLV	QAVD	QAVS	APSI-	APSI+	J
K	RMOD	VSSO	VDDO	RCA_ RPA	RDAT[5]	RDAT[1]	TTOHEN	TTOHCLK	TPOHFP	AVD[0]	AVS[0]	VDDO	VSSO	REFCLK	K
L	RVAL	RDAT[14]	RDAT[15]	RDAT[9]	RDAT[4]	RDAT[0]	TTOH	TTOHFP	TPOHCLK	TPOH	TRSTB	TDI	TMS	RALRM	L
M	RDAT[12]	RDAT[13]	VDDO	RDAT[8]	VDDO	TFPO	VDDO	VDDI	VDDO	TPOHEN	VDDO	TCK	TDO	TDCC	M
N	VSSQ	VSSO	VSSO	RDAT[7]	VSSO	RFPO	VSSO	VSSI	VSSO	RTOHCLK	VSSO	VSSO	RDCC	TDCLK	N
P	VDDQ	RDAT[11]	RDAT[10]	RDAT[6]	RDAT[3]	RCLK	TCLK	TFPI	RTOH	RTOHFP	RPOH	RPOHCLK	RPOHFP	RDCLK	P
	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

9 Pin Descriptions

9.1 Serial Line Side Interface Signals

Pin Name	Type	Pin No.	Function
SPECLV	Input	J6	The serial line PECL signal voltage select (SPECLV) selects between 3.3V PECL signaling and 5V PECL signaling for the serial line interface PECL input (RXD+/- and SD). When SPECLV is low, the PECL inputs expect a 5V PECL signal. When SPECLV is high, the PECL inputs expect a 3.3V PECL signal. Please refer to the Operation section for a discussion of PECL interfacing issues.
SDTTL	Input	E4	The signal detect voltage select (SDTTL) selects between PECL signaling and TTL signal for the signal detector inputs (SD). When SDTTL is low, the signal detect input expect PECL signal levels. When SDTTL is high, the signal detect input expect TTL signal level. Please refer to the Operation section for a discussion of PECL interfacing issues.
RXD+ RXD-	Differential PECL Input	H1 H2	The receive differential data PECL inputs (RXD+/-) contain the NRZ bit serial receive stream. The receive clock is recovered from the RXD+/- bit stream. Each differential input is terminated with an internal 100 ohm resistor. Please refer to the Operation section for a discussion of PECL interfacing issues.
SD	PECL Input	H3	The receive signal detect PECL inputs (SD) indicates the presence of valid receive signal power from the Optical Physical Medium Dependent Device. When SDTTL is low, a PECL logic high indicates the presence of valid data. A PECL logic low indicates a loss of signal. When SDTTL is high, a TTL logic high indicates the presence of valid data. A TTL logic low indicates a loss of signal. Please refer to the Operation section for a discussion of PECL interfacing issues
TXD+ TXD-	Differential Output	F1 F2	The transmit differential data PECL outputs (TXD+/) contain the 155.52 Mbit/s transmit stream. The TXD+/- outputs are driven using the synthesized clock from the CSU. The TXD+/- are differential TTL outputs which are converted to PECL levels using external passive networks. Please refer to the Operation section for a discussion of PECL interfacing issues.
REFCLK	Input	K1	The reference clock input (REFCLK) is a 19.44 MHz reference clock for both the clock recovery and the clock synthesis circuits. The REFCLK input is a single ended TTL input. For jitter requirements see Table 27.

9.2 Serial APS Interface Signals

Pin Name	Type	Pin No.	Function
APECLV	Input	J5	The APS PECL signal voltage select (APECLV) selects between 3.3V PECL signaling and 5V PECL signaling for the APS (APSI+/-) PECL inputs. When APECLV is low, the APSI+/- inputs expect a 5V PECL signal. When APECLV is high, these PECL inputs expect a 3.3V PECL signal. Please refer to the Operation section for a discussion of PECL interfacing issues.
APSI+ APSI-	Differential PECL Input	J1 J2	The receive APS differential data PECL inputs (APSI+/-) contain the NRZ bit serial APS stream. The receive clock is recovered from the APS+/- bit stream. Please refer to the Operation section for a discussion of PECL interfacing issues and APS functionality.
APSO+ APSO-	Differential PECL Output	D1 D2	The transmit APS differential data PECL outputs (APSO+/-) contain the 155.52 Mbit/s transmit APS stream. The APSO+/- outputs are driven using the synthesized clock from the clock synthesis unit. Please refer to the Operation section for a discussion of PECL interfacing issues and APS functionality.

9.3 Clocks and Alarms Signals

Pin Name	Type	Pin No.	Function
RALRM	Output	L1	The receive alarm (RALRM) outputs indicates the state of the receive framing. RALRM is low if no receive alarms are active. RALRM is optionally high if line AIS (LAIS), path AIS (PAIS), line RDI (LRDI), path RDI (PRDI), enhanced path RDI (PERDI), loss of signal (LOS), loss of frame (LOF), out of frame (OOF), loss of pointer (LOP), loss of pointer concatenation (LOPC/AISC), loss of cell delineation (LCD), signal fail BER (SFBER), signal degrade BER (SDBER), path trace identification mismatch (TIM) or path signal label mismatch (PSLM) is detected . RALARM is an asynchronous output with a minimum period of one RCLK clock.
RCLK	Output	P9	The receive clock (RCLK) provides a timing reference for the S/UNI-1x155 receive function outputs. RCLK is a 19.44 MHz, 50% duty cycle clock.
RFPO	Output	N9	The receive frame pulse output (RFPO), when the framing alignment has been found (the OOF register bit is low), is an 8 kHz signal derived from the receive clock RCLK. RFPO pulses high for one RCLK cycle every 2430 RCLK cycles. RFPO is updated on the rising edge of RCLK.
TCLK	Output	P8	The transmit clock (TCLK) provides timing for the S/UNI-1x155 transmit function operation for a channel. TCLK is a 19.44 MHz, 50% duty cycle clock.
TFPO	Output	M9	The active-high framing position output (TFPO) signal is an 8 kHz signal derived from the transmit clock TCLK. TFPO pulses high for one TCLK cycle every 2430 TCLK cycles. TFPO is updated on the rising edge of TCLK.
TFPI	Input	P7	The active high framing position (TFPI) signal is an 8 kHz timing marker for the transmitter. TFPI is used to align the SONET/SDH transport frame generated by the S/UNI-1x155 device to a system reference. TFPI should be brought high for a single TCLK period every 2430 (+/-1) TCLK cycles or a multiple thereof. TFPI must be tied low if such synchronization is not required. By design, TFPI has a built-in +/- 1 cycle tolerance. TFPI is sampled on the rising edge of TCLK.
XOFF	Input	G9	The transmit off (XOFF) input prevents the transmission of cells and packet data from the transmit FIFO. For ATM applications, the next cell transmitted is an idle/unassigned cell regardless of the number of cells in the FIFO when XOFF is set high. Idle/unassigned cells are transmitted until XOFF is deasserted. For POS applications, this signal is ignored. XOFF may be treated as an asynchronous signal. XOFF must be tied low if it is not used.

9.4 Section and Line Status DCC Signals

Pin Name	Type	Pin No.	Function
RDCLK	Output	P1	The receive DCC clock (RDCLK) is the clock used to update the associated RDCC outputs. When the channel DCC output is configured for section DCC, the associated RDCLK is a 192 kHz clock generated by gapping a 216 kHz clock. When the channel DCC output is configured for line DCC, the associated RDCLK is a 576 kHz clock generated by gapping a 2.16 MHz clock.
RDCC	Output	N2	The receive DCC (RDCC) signals contain the serial data communication channels extracted from the incoming stream. When configured for section DCC, the associated RDCC output is the extracted section DCC bytes (D1, D2, D3). When configured for line DCC, the associated RDCC output is the extracted line DCC bytes (D4 - D12). RDCC is updated on the falling edge of the associated
TDCLK	Output	N1	The transmit DCC clocks (TDCLK) is the clock used to sample the associated TDCC inputs. When the channel DCC input is configured for section DCC, the associated TDCLK is a 192 kHz clock generated by gapping a 216 kHz clock. When the channel DCC input is configured for line DCC, the associated TDCLK is a 576 kHz clock generated by gapping a 2.16 MHz clock.
TDCC	Input	M1	The transmit DCC (TDCC) signals contain the serial data communication channels. When not used, these inputs should be connected to logic zero. When configured for section DCC, the value sampled on the TDCC input is inserted into the associated section DCC bytes (D1, D2, D3). When configured for line DCC, the value sampled on the TDCC input is inserted into the associated line DCC bytes (D4 – D12). TDCC is sampled on the rising edge of the associated TDCLK.

9.5 Transmit and Receive Overhead Insertion and Extraction Interfaces

Pin Name	Type	Pin No.	Function
TTOH	Input	L8	The transmit transport overhead input (TTOH) contains the transport overhead bytes which may be inserted into the transmit stream. Insertion is controlled by the TTOHEN input. TTOH is sampled on the rising edge of TTOHCLK.
TTOHEN	Input	K8	The transmit transport overhead insert enable (TTOHEN) signal, together with internal register bits, controls the source of the transport overhead data which is transmitted. While TTOHEN is high during the first bit of the byte to be inserted, values sampled on the TTOH input are inserted into the corresponding transport overhead bit position. While TTOHEN is low, default values are inserted into these transport overhead bit positions. TTOHEN is sampled on the rising edge of TTOHCLK.
TTOHFP	Output	L7	The transmit transport overhead frame position (TTOHFP) signal is used to locate the individual transport overhead bits in the transport overhead input (TTOH). TTOHFP is set high while bit 1 (the most significant bit) of the first framing byte (A1) is expected on TTOH. TTOHFP is updated on the falling edge of TTOHCLK.
TTOHCLK	Output	K7	The transmit transport overhead clock (TTOHCLK) is nominally a 5.184 MHz clock which provides timing for circuitry that sources the transport overhead stream (TTOH). TTOHCLK is derived from a gapped 6.48 MHz clock.
TPOH	Input	L5	The transmit path overhead data (TPOH) signal contains the path overhead bytes and error masks (B3) which may be inserted, or used to insert path BIP-8 errors into the path overhead byte positions in the transmit stream. Insertion is controlled by the TPOHEN input, or by bits in internal registers. TPOH is sampled on the rising edge of TPOHCLK.
TPOHEN	Input	M5	The transmit path overhead insert enable (TPOHEN) signal, together with internal register bits, controls the source of the path overhead data which is transmitted. While TPOHEN is high, values sampled on the TPOH input are inserted into the corresponding path overhead bit position. While TPOHEN is low, values obtained from internal registers are inserted into these path overhead bit positions. A high level on TPOHEN during the B3 bit positions enables an error mask. While the error mask is enabled, a high level on input TPOH causes the corresponding B3 bit position to be inverted. A low level on TPOH allows the corresponding bit position to pass through the S/UNI-1x155 uncorrupted. TPOHEN is sampled on the rising edge of TPOHCLK.

Pin Name	Type	Pin No.	Function
TPOHFP	Output	K6	The transmit path overhead frame position (TPOHFP) signal may be used to locate the individual path overhead bits in the path overhead data stream (TPOH). TPOHFP is logic one while bit 1 (the most significant bit) of the path trace byte (J1) is expected in the TPOH stream. TPOHFP is updated on the falling edge of TPOHCLK.
TPOHCLK	Output	L6	The transmit path overhead clock (TPOHCLK) is nominally a 576 kHz clock which provides timing for circuitry that sources the path overhead stream, TPOH. TPOHCLK is derived from a gapped 810 KHz clock.
RTOH	Output	P6	The receive transport overhead output (RTOH) contains the entire receive transport overhead extracted from the receive stream. RTOH is updated on the falling edge of RTOHCLK.
RTOHFP	Output	P5	The receive transport overhead frame position (RTOHFP) signal is used to locate the individual receive transport overhead bits in the transport overhead output (RTOH). RTOHFP is set high while bit 1 (the most significant bit) of the first framing byte (A1) is present in the RTOH stream. RTOHFP is updated on the falling edge of RTOHCLK.
RTOHCLK	Output	N5	The receive transport overhead clock (RTOHCLK) is nominally a 5.184 MHz clock which provides timing to process the extracted receive transport overhead. RTOHCLK is derived from a gapped 6.48 MHz clock.
RPOH	Output	P4	The receive path overhead data (RPOH) signal contains the path overhead bytes extracted from the received SONET/SDH frame. RPOH is updated on the falling edge of RPOHCLK.
RPOHFP	Output	P2	The receive path overhead frame position (RPOHFP) signal may be used to locate the individual receive path overhead bits in the path overhead data stream (RPOH). RPOHFP is logic one while bit 1 (the most significant bit) of the path trace byte (J1) is present in the RPOH stream. RPOHFP is updated on the falling edge of RPOHCLK.
RPOHCLK	Output	P3	The receive path overhead clock (RPOHCLK) is nominally a 576 kHz clock which provides timing to process the extracted receive path overhead. RPOHCLK is derived from a gapped 648 KHz clock.

9.6 Transmit ATM (UTOPIA) and Packet over SONET/SDH (POS) System Interface

Pin Name	Type	Pin No.	Function
TFCLK	Input	F14	The UTOPIA transmit FIFO write clock (TFCLK) is used to write ATM cells to the cell transmit FIFO. In UTOPIA operation, TFCLK must cycle at a 52 MHz to 25 MHz instantaneous rate, and must be a free running clock (cannot be gapped).
			The POS-PHY transmit FIFO write clock (TFCLK) is used to write packet data into the packet FIFO. In POS-PHY operation, TFCLK must cycle at a 52 MHz to 25 MHz instantaneous rate, and must be a free running clock (cannot be gapped).
TDAT[0] TDAT[1] TDAT[2] TDAT[3] TDAT[4] TDAT[5] TDAT[6] TDAT[7] TDAT[8] TDAT[9] TDAT[10] TDAT[11] TDAT[12] TDAT[13] TDAT[14] TDAT[15]	Input	C14 B14 B13 A14 A13 A12 B12 A11 B11 C11 A10 D10 A9 B9 C9 D9	The UTOPIA transmit cell data (TDAT[15:0]) bus carries the ATM cell octets that are written to the transmit FIFO. In UTOPIA operation, the TDAT[15:0] bus is considered valid only when TENB is simultaneously asserted. TDAT[15:0] is sampled on the rising edge of TFCLK.
			The POS-PHY transmit packet data (TDAT[15:0]) bus carries the POS packet octets that are written to the transmit FIFO. In POS-PHY operation, the packet data sample on TDAT[15:0] is considered valid when TENB is sampled low. TDAT[15] is the first bit transmitted and TDAT[0] is the last bit transmitted. TDAT[15:0] is sampled on the rising edge of TFCLK.
TPRTY	Input	E9	The UTOPIA transmit bus parity (TPRTY) signal indicates the parity on the TDAT[15:0] bus. A parity error is indicated by a status bit and a maskable interrupt. Cells with parity errors are inserted in the transmit stream, so the TPRTY input may be unused. TPRTY is considered valid only when TENB is simultaneously asserted. TPRTY is sampled on the rising edge of TFCLK.
			The POS-PHY transmit bus parity (TPRTY) signal indicates the parity on the TDAT[15:0] bus. A parity error is indicated by a status bit and a maskable interrupt. Packets with parity errors are inserted in the transmit stream, so the TPRTY input may be unused. TPRTY is considered valid only when TENB is simultaneously asserted. TPRTY is sampled on the rising edge of TFCLK.

Pin Name	Type	Pin No.	Function
TENB	Input	C13	The UTOPIA transmit write enable (TENB) signal is an active low input which is used to initiate writes to the transmit FIFOs. When TENB is sampled high, the data sampled on TDAT[15:0], TRPTY and TSOC is invalid. When TENB is sampled low, the information sampled on TDAT[15:0], TPRTY and TSOC is valid and is written into the FIFO. A high to low transition on TENB is needed in conjunction with TADR[4:0] to select the transmit PHY. TENB is sampled on the rising edge of TFCLK.
			The POS-PHY transmit write enable (TENB) signal is an active low input which is used to initiate writes to the transmit FIFOs. When TENB is sampled high, the information sampled on TDAT[15:0], TPRTY, TSOP, TEOP, TMOD and TERR is invalid. When TENB is sampled low, the information sampled on TDAT[15:0], TPRTY, TSOP, TEOP, TMOD and TERR is valid and is written into the FIFO. TENB is sampled on the rising edge of TFCLK.
TSOC	Input	E14	The UTOPIA transmit start of cell (TSOC) signal marks the start of a cell structure on the TDAT[15:0] bus. When TSOC is sampled high, the first word of the ATM cell structure is sampled on the TDAT[15:0] bus. TSOC should be present for each cell structure. TSOC is considered valid only when TENB is simultaneously asserted. TSOC is sampled on the rising edge of TFCLK.
TSOP			The POS-PHY transmit start of packet (TSOP) signal indicates the start of a packet on the TDAT[15:0] bus. When TSOP is sampled high, the first word of the packet is sampled on TDAT[15:0] bus. TSOP is required to be present at all instances for proper operation. TSOP is considered valid only when TENB is simultaneously asserted. TSOP is sampled on the rising edge of TFCLK.
TEOP	Input	D14	The POS-PHY transmit end of packet (TEOP) marks the end of packet on the TDAT[15:0] bus when configured for packet data. TEOP sampled high indicates the last word of the packet is sampled on the TDAT[15:0] bus. The TMOD bus indicates how many valid bytes of packet data are in the last word. It is legal to set TSOC_TSOP high at the same time as TEOP is high in order to support one, two, three and four byte packets. TEOP is only valid when TENB is simultaneously asserted. TEOP is only used for POS-PHY operation and is sampled on the rising edge of TFCLK.

Pin Name	Type	Pin No.	Function
TERR	Input	C12	The POS-PHY transmit error (TERR) is used to indicate that the current packet must be aborted. Packets marked with TERR will be appended with the HDLC abort sequence (0x7D-0x7E) when transmitted. TERR sampled high when TEOP is sampled high marks the current packet to be aborted. TERR is only considered valid when TENB and TEOP are simultaneously asserted. TERR is only used for POS-PHY operation and is sampled on the rising edge of TFCLK.
TMOD	Input	D11	The POS-PHY transmit word modulo (TMOD) signal indicates the number of valid bytes of data on TDAT[15:0] during POS-PHY operation. The value sampled on the TMOD bus when TEOP is sampled high specifies the number of valid byte of packet data on TDAT[15:0]. TMOD = "0" TDAT[15:0] valid TMOD = "1" TDAT[15:8] valid TMOD is considered valid only when TENB and TEOP are simultaneously asserted. TMOD is only used for POS-PHY operation and is sampled on the rising edge of TFCLK.
TADR[0] TADR[1] TADR[2] TADR[3] TADR[4]	Input	E13 E12 F11 F10 F9	The UTOPIA transmit port address select (TADR[4:0]) is used to select the channel whose FIFO fill status is to be polled or the channel for which a UTOPIA cell transfer is desired. When TENB transitions from high to low, the value sampled on TADR[4:0] selects the channel FIFO to which the ATM cell is written. During all other conditions, the fill status of the channel FIFO with the address sampled on TADR[4:0] is reported on TCA on the following clock cycle. TADR[4:0] is sampled on the rising edge of TFCLK.
			The POS-PHY transmit port address select (TADR[4:0]) is used to select the channel whose FIFO fill status is to be polled. The address sampled on TADR[4:0] specifies the channel FIFO being polled. The PTPA output is updated on the following clock cycle with the channel's fill level based on the programmable thresholds. TADR[4:0] is sampled on the rising edge of TFCLK.
STPA	Output	E11	The POS-PHY selected transmit packet available (STPA) signal provides status indication of when cell space is available in the transmit FIFO. When STPA transitions high, it indicates that the transmit FIFO has enough room to store a configurable number of data bytes. When STPA transitions low, it indicates that the transmit FIFO is either full or near full. These thresholds are specified in the TFCLK DLL registers. STPA is updated on the rising edge of TFCLK.

Pin Name	Type	Pin No.	Function
TCA	Output	E10	The UTOPIA transmit cell available (TCA) signal provides status indication of when cell space is available in the transmit FIFO. TCA is used to poll the channel FIFOs to determine the number of free ATM cell buffers that are in the FIFO. The address sampled on TADR[4:0] will cause TCA to be updated with the channel information on the following clock cycle. When TCA is high, the channel FIFO can accept at least one more ATM cell. When TCA is low, the channel FIFO fill level exceeds the threshold specified by the FIFODP[1:0] register. Note that regardless of the threshold, a channel FIFO can store 16 ATM cells. TCA is updated on the rising edge of TFCLK.
PTPA			The POS-PHY polled transmit packet available (PTPA) signal provides status indication of when cell space is available in the transmit FIFO. The TADR[4:0] address is used to determine which channel to report on PTPA. When PTPA transitions high, it indicates that the transmit FIFO has enough room to store a configurable number of data bytes. When PTPA transitions low, it indicates that the transmit FIFO is either full or near full. These thresholds are specified in the TFCLK DLL registers. PTPA is updated on the rising edge of TFCLK.

9.7 Receive ATM (UTOPIA) and Packet over SONET/SDH (POS) System Interface

Pin Name	Type	Pin No.	Function
RFCLK	Input	G14	The UTOPIA receive FIFO read clock (RFCLK). is used to read ATM cells from the cell receive FIFO. In UTOPIA operation, RFCLK must cycle at a 52 MHz to 20 MHz instantaneous rate, and must be a free running clock (cannot be gapped).
			The POS-PHY receive FIFO read clock (RFCLK). is used to read packet data from the packet FIFO. In POS-PHY operation, RFCLK must cycle at a 52 MHz to 20 MHz instantaneous rate, and must be a free running clock (cannot be gapped).
RPRTY	Output	J11	The UTOPIA receive parity (RPRTY) signal indicates the parity of the RDAT[15:0] bus. Odd or even parity may be selected using software control. In UTOPIA operation, the value on RPRTY is updated on the following clock cycle when RENB is sampled low. RPRTY is updated on the rising edge of RFCLK.
			The POS-PHY receive parity (RPRTY) indicates the parity of the RDAT[15:0] bus. Odd or even parity may be selected using software control. In POS-PHY operation, the value on RPRTY is updated on the next clock cycle when RENB is sampled low. RPRTY is updated on the rising edge of RFCLK.
RDAT[0] RDAT[1] RDAT[2] RDAT[3] RDAT[4] RDAT[5] RDAT[6] RDAT[7] RDAT[8] RDAT[9] RDAT[10] RDAT[11] RDAT[12] RDAT[13] RDAT[14] RDAT[15]	Output	L9 K9 J9 P10 L10 K10 P11 N11 M11 L11 P12 P13 M14 M13 L13 L12	The UTOPIA receive cell data (RDAT[15:0]) bus carries the ATM cell octets that are read from the receive FIFO. In UTOPIA operation, RDAT[15:0] is updated on the following clock cycle after RENB is sampled low. RDAT[15:0] is updated on the rising edge of RFCLK.
			The POS-PHY receive packet data (RDAT[15:0]) bus carries the POS packet octets that are read from the receive FIFO. In POS-PHY operation, the packet data on RDAT[15:0] is updated on the following clock cycle when RENB is sampled low. RDAT[15] is the first bit received and RDAT[0] is the last bit received RDAT[15:0] is updated on the rising edge of RFCLK.

Pin Name	Type	Pin No.	Function
RENB	Input	J14	The UTOPIA receive read enable (RENB) is used to initiate reads from the receive FIFO. The system may de-assert RENB if it is unable to accept more cells. In UTOPIA operation, when RENB is sampled low, RDAT[15:0], RRPTY and RSOC are updated on the following RFCLK cycle. When RENB is sampled high, the information on RDAT[15:0], RPRTY and RSOC_RSOP is held on the next clock cycle. RENB is also used to select the channel to read data. When RENB transitions from high to low, the channel address on RADR[4:0] selects the channel to read from. RENB is sampled on the rising edge of RFCLK.
			The POS-PHY receive read enable (RENB) is used to initiate reads from the receive FIFO. During a data transfer, RVAL must be monitored since it will indicate if the data is valid. The system may deassert RENB at any time if it is unable to accept more data. In POS-PHY operation, the information on RDAT[15:0], RPRTY, RSOP, REOP, RMOD, RERR, and RVAL is held on the following clock cycle when RENB is sampled high. When RENB is sampled low, the values on RDAT[15:0], RPRTY, RSOP, REOP, RMOD, RERR, and RVAL are valid and are updated on the following clock cycle. RENB is sampled on the rising edge of RFCLK.
RSOC	Output	J10	The UTOPIA receive start of cell (RSOC) signal marks the start of a cell structure on the RDAT[15:0] bus. In UTOPIA operation, the first word of the cell structure is present on the RDAT[15:0] bus when RSOC is high. RSOC is updated on the following clock cycle when RENB is sampled low. RSOC is updated on the rising edge of RFCLK.
RSOP			The POS-PHY receive start of packet (RSOP) indicates the start of a packet on the RDAT[15:0] bus. In POS-PHY operation, the first word of the packet is on the RDAT[15:0] bus when RSOP is high. RSOP is updated on the following clock cycle when RENB is sampled low. RSOP is updated on the rising edge of RFCLK
REOP	Output	J12	The POS-PHY receive end of packet (REOP) marks the end of packet on the RDAT[15:0] bus. It is legal for RSOP to be high at the same time REOP is high. REOP set high indicates the last word of the packet is on the RDAT[15:0] bus. The RMOD bus indicates how many valid bytes of packet data are in the last word. It is legal for RSOP to be high at the same time as REOP is high in order to support one, two, three and four byte packets. The value on REOP is updated on the next clock cycle when RENB is sampled low. REOP is only used for POS-PHY operation and is updated on the rising edge of RFCLK.

Pin Name	Type	Pin No.	Function
RERR	Output	J13	The POS-PHY receive error (RERR) indicates that the current packet is invalid due to an error such as invalid FCS, excessive length or received HDLC abort sequence (0x7D-0x7E). RERR is high when REOP is high marking the current packet as erred. RERR is low when REOP is low. The value on RERR is updated on the next clock rising edge when RENB is sampled low. RERR is only used for POS-PHY operation and is updated on the rising edge of RFCLK.
RMOD	Output	K14	The POS-PHY receive modulo (RMOD) indicates the number of valid bytes of data on RDAT[15:0] during POS-PHY operation. The value on the RMOD bus when REOP is high specifies the number of valid bytes of packet data on RDAT[15:0]. RMOD is set to “0” when REOP is low. RMOD = "0" RDAT[15:0] valid RMOD = "1" RDAT[15:8] valid The value on RMOD is updated on the next clock rising edge when RENB is sampled low. RMOD is only used for POS-PHY operation and is updated on the rising edge of RFCLK.
RVAL	Output	L14	The POS-PHY receive data valid (RVAL) signal indicates the validity of the receive data signals. When RVAL is high, the receive signals RDAT, RSOP, REOP, RMOD, RPRTY and RERR are valid. When RVAL is low, all receive signals are invalid and must be disregarded. RVAL will transition low on a FIFO empty condition or on an end of packet. Once deasserted, RVAL will remain low until RENB is deasserted. No data will be removed from the receive FIFO while RVAL is held low. RVAL is tri-stated when RENB is deasserted. See Functional Timing section for more details on using RVAL with RPA. RVAL is updated on the rising edge of RFCLK.
RADR[0] RADR[1] RADR[2] RADR[3] RADR[4]	Input	G11 G10 H14 H11 H10	The UTOPIA receive port address select (RADR[4:0]) is used to select the channel whose FIFO fill status is to be polled or the channel for which a UTOPIA cell transfer is desired. When RENB transitions from high to low, the value sampled on RADR[4:0] selects the channel FIFO from which the ATM cell is read. During all other conditions, the fill status of the channel FIFO with the address sampled on RADR[4:0] is reported on RCA. RADR[4:0] is sampled on the rising edge of RFCLK.
			The POS-PHY receive port address select (RADR[4:0]) is used to select the channel whose FIFO fill status is to be polled or the channel for which packet data is desired. When RENB transitions from high to low, the value sampled on RADR[4:0] selects the channel FIFO from which packet data is read. During all other conditions, the fill status of the channel FIFO with the address sampled on RADR[4:0] is reported on RPA. RADR[4:0] is sampled on the rising edge of RFCLK.

Pin Name	Type	Pin No.	Function
RCA	Output	K11	The UTOPIA receive cell available (RCA) is used to determine the fill status of each channel FIFO during UTOPIA operation. RCA is used to poll the channel FIFOs to determine the number of ATM cells that are in the FIFO. The address sampled on RADR[4:0] will cause RCA to be updated with the channel information on the following clock cycle. When RCA is set high, the channel FIFO has at least one complete ATM cell. When RCA is set low, the channel FIFO does not contain a complete ATM cell. RCA is updated on the rising edge of RFCLK.
RPA			The POS-PHY receive packet available (RPA) provides a direct status indication of when a programmable number of bytes of data is available in the receive FIFO. The receive FIFO has at least one end of packet or a programmable minimum number of bytes to be read when RPA is high. RPA is otherwise low. The threshold is configured in the RXFP registers. The RPA may incorrectly indicate the FIFO fill level is above the high water mark after an end of packet is transferred over RDAT[15:0]. See the Functional Timing section for more details of using RVAL with RPA to prevent data corruption. RPA is updated on the rising edge of RFCLK.

9.8 Microprocessor Interface Signals

Pin Name	Type	Pin No.	Function
CSB	Input	A2	The active-low chip select (CSB) signal is low during S/UNI-1x155 register accesses. When CSB is high, the RDB and WRB inputs are ignored. When CSB is low, the RDB and WRB are valid. CSB must be high when RSTB is low to properly reset the chip. If CSB is not required (i.e., registers accesses are controlled using the RDB and WRB signals only), CSB must be connected to an inverted version of the RSTB input.
RDB	Input	A3	The active-low read enable (RDB) signal is low during S/UNI-1x155 register read accesses. The S/UNI-1x155 drives the D[7:0] bus with the contents of the addressed register while RDB and CSB are low.
WRB	Input	B2	The active-low write strobe (WRB) signal is low during a S/UNI-1x155 register write accesses. The D[7:0] bus contents are clocked into the addressed register on the rising WRB edge while CSB is low.
D[0] D[1] D[2] D[3] D[4] D[5] D[6] D[7]	I/O	A8 D8 E8 A7 B7 C7 D7 E7	The bi-directional data bus D[7:0] is used during S/UNI-1x155 register read and write accesses.
A[0] A[1] A[2] A[3] A[4] A[5] A[6] A[7] A[8]	Input	F6 E6 D6 A6 E5 D5 C5 B5 A5	The address bus A[8:0] selects specific registers during S/UNI-1x155 register accesses.
A[9]	Input	D4	The test register select (A[9]) signal selects between normal and test mode register accesses. A[9] is high during test mode register accesses, and is low during normal mode register accesses. A[9] may be tied low.
RSTB	Input	B3	The active-low reset (RSTB) signal provides an asynchronous S/UNI-1x155 reset. RSTB is a Schmitt triggered input with an integral pull-up resistor. CSB must be held high when RSTB is low in order to properly reset this chip.
ALE	Input	A4	The address latch enable (ALE) is active-high and latches the address bus A[8:0] when low. When ALE is high, the internal address latches are transparent. It allows the S/UNI-1x155 to interface to a multiplexed address/data bus. ALE has an integral pull-up resistor.

Pin Name	Type	Pin No.	Function
INTB	Output	C3	The active-low interrupt (INTB) signal is set low when a S/UNI-1x155 interrupt source is active and that source is unmasked. The S/UNI-1x155 may be enabled to report many alarms or events via interrupts. Examples of interrupt sources are loss of signal (LOS), loss of frame (LOF), line AIS, line remote defect indication (LRDI) detect, loss of pointer (LOP), path AIS, path remote defect indication and others. INTB is tri-stated when the all enabled interrupt sources are acknowledged via an appropriate register access. INTB is an open drain output.
POS_ ATMB	Input	J8	The physical layer select (POS_ATMB) pin selects between the ATM and Packet over SONET/SDH modes of operation. When tied low, the device implements the ATM physical layer. The system interface operates UTOPIA Level 2 mode. When tied high, the device implements the Packet over SONET/SDH physical layer. The system interface operates in 16-bit POS-PHY Level 2 mode. This pin affects SONET/SDH mapping as well as the pin definitions of the system interface bus.
TSEN	Input	F7	The tristate enable (TSEN) signal allows tristate control over outputs RDAT[15:0], RPRTY, RSOC/RSOP, REOP, RMOD, RERR, RCA/RPA, RVAL, TCA/PTPA and STPA. When TSEN is high, the active low receive read enable input, RENB controls when outputs RDAT[15:0], RPRTY, RSOC/RSOP, REOP, RMOD, RERR are driven. Also, when TSEN is high, the TCA/PTPA and RCA/RPA are controlled by TADR[4:0] and RADR[4:0] respectively. When TSEN is low, all tristatable outputs are always driven.

9.9 JTAG Test Access Port (TAP) Signals

Pin Name	Type	Pin No.	Function
TCK	Input	M3	The test clock (TCK) signal provides clock timing for test operations that are carried out using the IEEE P1149.1 test access port. This pin has an internal pull-up resistor.
TMS	Input	L2	The test mode select (TMS) signal controls the test operations that are carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull-up resistor.
TDI	Input	L3	The test data input (TDI) signal carries test data into the S/UNI-1x155 via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull-up resistor.
TDO	Output	M2	The test data output (TDO) signal carries test data out of the S/UNI-1x155 via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tri-state output which is inactive except when shifting boundary scan data is in progress.
TRSTB	Input	L4	The active-low test reset (TRSTB) signal provides an asynchronous S/UNI-1x155 test access port reset via the IEEE P1149.1 test access port. TRSTB is a Schmitt triggered input with an integral pull-up resistor. Note that when not being used, TRSTB may be tied low or connected to the RSTB input.

9.10 Power and Ground

Pin Name	Type	Pin No.	Function
ATP	Analog	H6	The analog test port (ATP) is used for manufacturing testing only and should be tied to the analog ground plane (AVS).
AVD[0] AVD[1]	Analog Power	K5 H5	The analog power (AVD[1:0]) pins for the analog core. The AVD pins should be connected through passive filtering networks to a well-decoupled +3.3V analog power supply. Please see the Operation section for detailed information.
AVS[0] AVS[1]	Analog Ground	K4 H4	The analog ground (AVS[1:0]) pins for the analog core. The AVS pins should be connected to the analog ground of the analog power supply. Please see the Operation section for detailed information.
QAVD	Quiet Analog Power	J4	The quiet analog power (QAVD) pin for the analog core. The QAVD pin should be connected to a well-decoupled +3.3V analog power supply. Please see the Operation section for detailed information.
QAVS	Quiet Analog Ground	J3	The analog ground (QAVS) pins for the analog core. The AVS pins should be connected to the analog ground of the analog power supply. Please see the Operation section for detailed information.
VDDI	Digital Power	C8 G12 F5 M7	The core digital power (VDDI) pins should be connected to a well-decoupled +2.5 V digital power supply.
VSSI	Digital Power	B8 G13 G5 N7	The core digital ground (VSSI) pins should be connected to the digital group of the digital power supply.
VDDQ	Digital Power	A1 P14	The quiet I/O digital power (VDDQ) pins should be connected to a well-decoupled +3.3 V digital power supply.
VSSQ	Digital Power	B1 N14	The quiet I/O digital ground (VSSQ) pins should be connected to the digital group of the digital power supply.

Pin Name	Type	Pin No.	Function
VDDO	Digital Power	C1 C4 C6 C10 D12 E1 E3 F3 F12 G1 G3 H12 K3 K12 M4 M6 M8 M10 M12	The I/O digital power (VDDO) pins should be connected to a well-decoupled +3.3 V digital power supply.
VSSO	Digital Ground	B4 B6 B10 C2 D3 D13 E2 F4 F13 G2 G4 H13 K2 K13 N3 N4 N6 N8 N10 N12 N13	The I/O digital ground (VSSO) pins should be connected to the digital ground of the digital power supply.

9.11 No Connects

Pin Name	Type	Pin No.	Function
NC	Thermal No Connects	F8 G6 G7 G8 H7 H8 H9 J7	The normally open connections (NC) pins do not have any electrical connection in the device. However, these pins must be thermally connected to a thermal ground (for instance, a power or ground plane on the printed circuit board) to maintain the device's thermal characteristics.

Notes on Pin Description:

1. All digital inputs and bi-directional signals present minimum capacitive loading and operate at TTL logic levels except the inputs marked as Analog or differential pseudo-ECL (PECL).
2. All digital outputs and bi-directional signals have 8mA drive strength.
3. The differential pseudo-ECL inputs and outputs should be terminated in a passive network and interface at PECL levels as described in the Operation section.
4. It is mandatory that every digital ground pin (VSSI, VSSQ and VSSO) be connected to the printed circuit board ground plane to ensure reliable device operation.
5. It is mandatory that every digital power pin (VDDI, VDDQ and VDDO) be connected to printed circuit board power planes to ensure reliable device operation.
6. All analog power and ground pins can be sensitive to noise. They must be isolated from the digital power and ground. Care must be taken to correctly decouple these pins. Please refer to the Operation section and the S/UNI-1x155 reference design (PMC-2011618) for more information.
7. Due to ESD protection structures in the pads it is necessary to exercise caution when powering a device up or down. ESD protection devices behave as diodes between power supply pins and from I/O pins to power supply pins. Under extreme conditions it is possible to damage these ESD protection devices or trigger latch up. Please adhere to the recommended power supply sequencing as described in the Operation section of this document.

10 Functional Description

10.1 Receive Line Interface (CRSI)

The Receive Line Interface allows direct interface of the S/UNI-1x155 to optical modules (ODLs) or other medium interfaces. This block performs clock and data recovery on the incoming 155.52 Mbit/s data stream and SONET/SDH A1/A2 pattern framing.

10.1.1 Clock Recovery

The clock recovery units recovers the clock from each incoming bit serial data stream and is compliant with SONET and SDH jitter tolerance requirements. The clock recovery units utilize a low frequency reference clock to train and monitor its clock recovery PLL. Under loss of transition conditions, the clock recovery unit continues to output a line rate clock that is locked to this reference for keep alive purposes. The clock recovery unit utilizes a 19.44 MHz reference clock. The clock recovery unit provides status bits that indicate whether it is locked to data or the reference and also supports diagnostic loopback and a loss of signal input that squelches normal input data.

Initially upon start-up, the PLL locks to the reference clock, REFCLK. When the frequency of the recovered clock is within 488 ppm of the reference clock, the PLL attempts to lock to the data. Once in data lock, the PLL reverts to the reference clock if no data transitions occur in 96 bit periods or if the recovered clock drifts beyond 488 ppm of the reference clock.

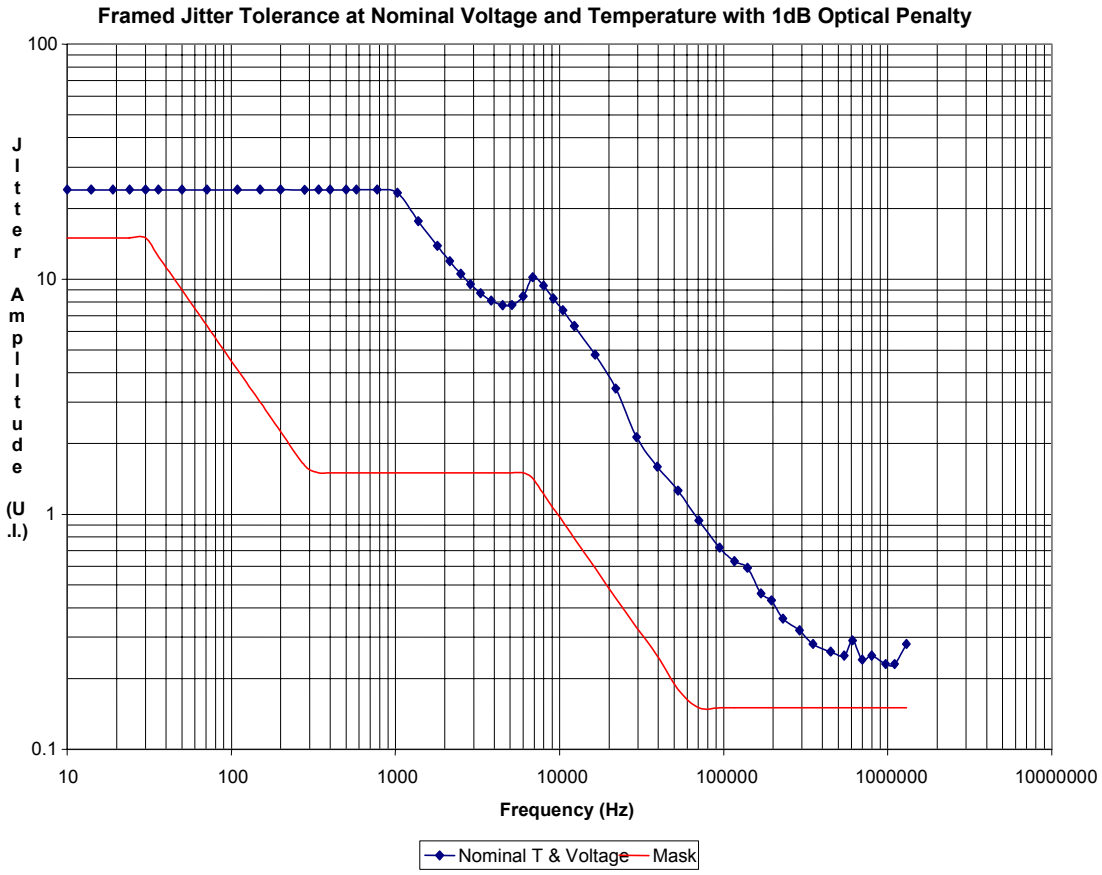
When the transmit clock is derived from the recovered clock (loop timing), the accuracy of the transmit clock is directly related to the REFCLK reference accuracy in the case of a loss of transition condition. To meet the Bellcore GR-253-CORE SONET Network Element free-run accuracy specification, the reference must be within +/-20 ppm. For LAN applications, the REFCLK accuracy may be relaxed to +/-50 ppm.

The loop filter transfer function is optimized to enable the PLL to track the jitter, yet tolerate the minimum transition density expected in a received SONET/SDH data signal. The total loop dynamics of the clock recovery PLL yield a jitter tolerance that exceeds the minimum tolerance specified for SONET/SDH equipment by GR-253-CORE (2000). Jitter transfer is measured using the GR-253-CORE (1995) requirement criteria.

The typical jitter tolerance performance of a S/UNI-1x155 channel is shown in Figure 3 with the GR-253-CORE jitter tolerance specification limits. The jitter tolerance setup used an AGILENT HFBR-5905 multi-mode fiber optic transceiver with approximately -10 dBm input power.

Note that for frequencies below 300Hz, the jitter tolerance is greater than 22 UIpp; 22 UIpp is the maximum jitter tolerance of the test equipment. The dip in the jitter tolerance curve between 10 kHz and 30 kHz is due to the clock difference detector.

Figure 3 Typical STS-3c/STM-1 S/UNI-1x155 Jitter Tolerance



10.1.2 Serial to Parallel Converter

The Serial to Parallel Converters (SIPO) convert each received bit serial stream to a byte serial stream. The SIPO searches for the initial SONET/SDH framing pattern in the receive stream, and performs serial to parallel conversion on octet boundaries.

While out of frame, the CRSI block monitors the bit-serial STS-3c/STM-1 data stream for an occurrence of an A1 byte. The CRSI adjusts its byte alignment of the serial-to-parallel converter when three consecutive A1 bytes followed by three consecutive A2 bytes occur in the data stream. The CRSI informs the RSOP Framer block when this framing pattern has been detected to reinitializes the RSOP to the new frame alignment.

While in frame, the CRSI maintains the byte alignment of the serial-to-parallel converter until RSOP declares out of frame.

10.2 Receive Section Overhead Processor (RSOP)

The Receive Section Overhead Processor (RSOP) provides frame synchronization, descrambling, section level alarm and performance monitoring. In addition, it may extract the section data communication channel from the section overhead and provide it serially on the receive DCC outputs.

10.2.1 Framer

The Framer Block determines the in-frame/out-of-frame status of the receive stream. While in-frame, the framing bytes (A1, A2) in each frame are compared against the expected pattern. Out-of-frame is declared when four consecutive frames containing one or more framing pattern errors have been received.

While out of frame, the CRSI block monitors the bit-serial STS-3c/STM-1 data stream for an occurrence of the framing pattern (A1, A2). The CRSI informs the RSOP Framer block when three A1 bytes followed by three A2 bytes has been detected to reinitializes the frame byte counter to the new alignment. The Framer block declares frame alignment on the next SONET/SDH frame when either all A1 and A2 bytes are seen error-free or when only the first A1 byte and the first four bits of the last A2 byte are seen error-free depending upon the selected framing algorithm.

Once in frame, the Framer block monitors the framing pattern sequence and declares out of frame (OOF) when one or more bit errors in each framing pattern are detected for four consecutive frames. Again, depending upon the algorithm either all framing bytes are examined for bit errors each frame, or only the first A1 byte and the first four bits of the last A2 byte are examined for bit errors each frame.

10.2.2 Descramble

The Descramble Block utilizes a frame synchronous descrambler to process the receive stream. The generating polynomial is $x^7 + x^6 + 1$ and the sequence length is 127. Details of the descrambling operation are provided in the references. Note that the framing bytes (A1 and A2) and the trace/growth bytes (J0/Z0) are not descrambled. A register bit is provided to disable the descrambling operation.

10.2.3 Data Link Extract

The Data Link Extract Block extracts the section data communication channel (bytes D1, D2, and D3) from an STS-3c/STM-1 stream. The extracted bytes are serialized and are output on the associated RDCC signal at a nominal 192 kbit/s rate. Timing for downstream processing of the data communication channel is provided by the RDCLK signal that is also output by the Data Link Extract Block. RDCLK is derived from a 216 kHz clock that is gapped to yield an average frequency of 192 kHz. RDCC is updated with timing aligned to RDCLK.

10.2.4 Error Monitor

The Error Monitor Block calculates the received section BIP-8 error detection code (B1) based on the scrambled data of the complete STS-3c/STM-1 frame. The section BIP-8 code is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 code is compared with the BIP-8 code extracted from the B1 byte of the following frame. Differences indicate that a section level bit error has occurred. Up to 64000 (8 x 8000) bit errors can be detected per second. The Error Monitor Block accumulates these section level bit errors in a 16-bit saturating counter that can be read via the microprocessor interface. Circuitry is provided to latch this counter so that its value can be read while simultaneously resetting the internal counter to 0 or 1, if appropriate, so that a new period of accumulation can begin without loss of any events. It is intended that this counter be polled at least once per second so as not to miss bit error events.

10.2.5 Loss of Signal

The Loss of Signal Block monitors the scrambled data of the receive stream for the absence of 1's or 0's. When 20 ± 3 µs of all zeros patterns or all ones patterns are detected, a loss of signal (LOS) is declared. Loss of signal is cleared when two valid framing words are detected and during the intervening time, no loss of signal condition is detected. The LOS signal is optionally reported on the RALRM output pin when enabled by the LOSEN Receive Alarm Control Register bit.

10.2.6 Loss of Frame

The Loss of Frame Block monitors the in-frame / out-of-frame status of the Framer Block. A loss of frame (LOF) is declared when an out-of-frame (OOF) condition persists for 3 ms. The LOF is cleared when an in-frame condition persists for a period of 3 ms. To provide for intermittent out-of-frame (or in-frame) conditions, the 3 ms timer is not reset to zero until an in-frame (or out-of-frame) condition persists for 3 ms. The LOF and OOF signals are optionally reported on the RALRM output pin when enabled by the LOFEB and OOFEN Receive Alarm Control Register bits.

10.3 Receive Line Overhead Processor (RLOP)

The Receive Line Overhead Processor (RLOP) provides line level alarm and performance monitoring. In addition, it may extract the line data communication channel from the line overhead and provide it serially on the receive DCC outputs.

10.3.1 Line RDI Detect

The Line RDI Detect Block detects the presence of Line Remote Defect Indication (LRDI) in the receive stream. Line RDI is declared when a 110 binary pattern is detected in bits 6, 7, and 8 of the K2 byte, for three or five consecutive frames. Line RDI is removed when any pattern other than 110 is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. The LRDI signal is optionally reported on the RALRM output pin when enabled by the LRDIEN Receive Alarm Control Register bit.

10.3.2 Line AIS Detect

The Line AIS Block detects the presence of a Line Alarm Indication Signal (LAIS) in the receive stream. Line AIS is declared when a 111 binary pattern is detected in bits 6, 7, and 8 of the K2 byte, for three or five consecutive frames. Line AIS is removed when any pattern other than 111 is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. The LAIS signal is optionally reported on the RALRM output pin when enabled by the LAISEN Receive Alarm Control Register bit.

10.3.3 Data Link Extract Block

The Data Link Extract Block extracts the line data communication channel (bytes D4 to D12) fromthe STS-3c/STM-1 stream. The extracted bytes are serialized and output on the associated RDCC output at a nominal 576 kbit/s rate. Timing for downstream processing of the data communication channel is provided by the RDCLK output. RDCLK is derived from a 2.16 MHzclock that is gapped to yield an average frequency of 576 kHz.

10.3.4 Error Monitor Block

The Error Monitor Block calculates the received line BIP-8 error detection codes based on the Line Overhead bytes and synchronous payload envelopes of the STS-3c/STM-1 stream. The line BIP-8 code is a bit interleaved parity calculation using even parity. Details are provided in the references. The calculated BIP-8 codes are compared with the BIP-8 codes extracted from the following frame. Any differences indicate that a line layer bit error has occurred. Optionally the RLOP can be configured to count a maximum of only one BIP error per frame.

This block also extracts the line FEBE code from the M1 byte. The FEBE code is contained in bits 2 to 8 of the M1 byte, and represents the number of line BIP-8 errors that were detected in the last frame by the far end. The FEBE code value has 25 legal values (0 to 24) for an STS-3c/STM-1 stream. Illegal values are interpreted as zero errors.

The Error Monitor Block accumulates B2 error events and FEBE events in two 20-bit saturating counters that can be read via the CBI. The contents of these counters may be transferred to internal holding registers by writing to any one of the counter addresses, or by using the TIP register bit feature. During a transfer, the counter value is latched and the counter is reset to 0 (or 1, if there is an outstanding event). Note, these counters should be polled at least once per second to avoid saturation.

The B2 error event counters optionally can be configured to accumulate only "word" errors. A B2 word error is defined as the occurrence of one or more B2 bit error events during a frame. The B2 error counter is incremented by one for each frame in which a B2 word error occurs.

In addition the FEBE events counters optionally can be configured to accumulate only "word" events. A FEBE word event is defined as the occurrence of one or more FEBE bit events during a frame. The FEBE event counter is incremented by one for each frame in which a FEBE event occurs. If the extracted FEBE value is in the range 1 to 4 the FEBE event counter will be incremented for each and every FEBE bit. If the extracted FEBE value is greater than 4 the FEBE event counter will be incremented by 4.

10.4 The Receive APS, Synchronization Extractor and Bit Error Monitor (RASE)

10.4.1 Automatic Protection Switch Control

The Automatic Protection Switch (APS) control block filters and captures the receive automatic protection switch channel bytes (K1 and K2) allowing them to be read via the RASE APS K1 Register and the RASE APS K2 Register. The bytes are filtered for three frames before being written to these registers. A protection switching byte failure alarm is declared when twelve successive frames have been received, where no three consecutive frames contain identical K1 bytes. The protection switching byte failure alarm is removed upon detection of three consecutive frames containing identical K1 bytes. The detection of invalid APS codes is done in software by polling the RASE APS K1 Register and the RASE APS K2 Register.

10.4.2 Bit Error Rate Monitor

The Bit Error Monitor Block (BERM) calculates the received line BIP-24 error detection code (B2) based on the line overhead and synchronous payload envelope of the receive data stream. The line BIP-24 code is a bit interleaved parity calculation using even parity. Details are provided in the references. The calculated BIP code is compared with the BIP-24 code extracted from the B2 bytes of the following frame. Any differences indicate that a line layer bit error has occurred. Up to 192,000 (24 BIP/frame x 8000 frames/second) bit errors can be detected per second for STS-3c/STM-1 rate.

The BERM accumulates these line layer bit errors in a 20 bit saturating counter that can be read via the microprocessor interface. During a read, the counter value is latched and the counter is reset to 0 (or 1, if there is an outstanding event). Note, this counter should be polled at least once per second to avoid saturation that in turn may result in missed bit error events.

The BERM block is able to simultaneously monitor for signal fail (SF) or signal degrade (SD) threshold crossing and provide alarms through software interrupts. The bit error rates associated with the SF or SD alarms are programmable over a range of 10^{-3} to 10^{-9}. Details are provided in the Operation section.

10.4.3 Synchronization Status Extraction

The Synchronization Status Extraction (SSE) Block extracts the synchronization status (S1) byte from the line overhead. The SSE block can be configured to capture the S1 nibble after three or after eight frames with the same value (filtering turned on) or after any change in the value (filtering turned off). The S1 nibble can be read via the CBI interface.

10.5 Receive Transport Overhead Extract Port

The Transport Overhead Extract Port extracts the entire receive transport overhead on RTOH for optional external transport overhead processing. RTOHFP is provided to identify the most significant bit of the A1 framing byte on RTOH. The transport overhead clock, RTOHCLK is nominally a 5.184 MHz clock. RTOH and RTOHFP are updated on the falling edge of RTOHCLK.

10.6 Receive Path Overhead Processor (RPOP)

The Receive Path Overhead Processor (RPOP) provides pointer interpretation, extraction of path overhead, extraction of the synchronous payload envelope, and path level alarm indication and performance monitoring.

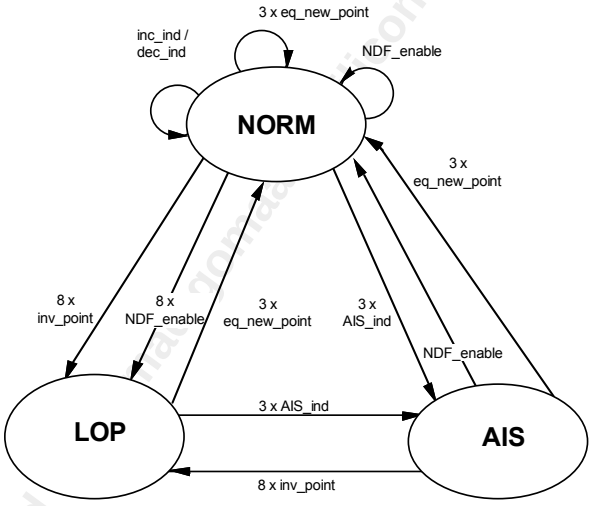
10.6.1 Pointer Interpreter

The Pointer Interpreter interprets the incoming pointer (H1, H2) as specified in the references. The pointer value is used to determine the location of the path overhead (the J1 byte) in the incoming STS-3c/STM-1 stream. The algorithm can be modeled by a finite state machine. Within the pointer interpretation algorithm three states are defined as shown below:

NORM_state (NORM)
AIS_state (AIS)
LOP_state (LOP)

The transition between states will be consecutive events (indications), e.g., three consecutive AIS indications to go from the NORM_state to the AIS_state. The kind and number of consecutive indications activating a transition is chosen such that the behavior is stable and insensitive to low BER. The only transition on a single event is the one from the AIS_state to the NORM_state after receiving a NDF enabled with a valid pointer value. It should be noted that, since the algorithm only contains transitions based on consecutive indications, this implies that, for example, non-consecutively received invalid indications do not activate the transitions to the LOP_state.

Figure 4 Pointer Interpretation State Diagram



The following table defines the events (indications) shown in the state diagram.

Table 2 Pointer Interpreter Event (Indications) Description

Event (Indication)	Description
norm_point	disabled NDF + ss + offset value equal to active offset
NDF_enable	enabled NDF + ss + offset value in range of 0 to 782 or enabled NDF + ss, if NDFPOR bit is set (Note that the current pointer is not updated by an enabled NDF if the pointer is out of range).
AIS_ind	H1 = 'hFF, H2 = 'hFF
inc_ind	disabled NDF + ss + majority of I bits inverted + no majority of D bits inverted + previous NDF_enable, inc_ind or dec_ind more than 3 frames ago
dec_ind	disabled NDF + ss + majority of D bits inverted + no majority of I bits inverted + previous NDF_enable, inc_ind or dec_ind more than 3 frames ago
inv_point	not any of above (i.e., not norm_point, and not NDF_enable, and not AIS_ind, and not inc_ind and not dec_ind)
new_point	disabled_NDF + ss + offset value in range of 0 to 782 but not equal to active offset
inc_req	majority of I bits inverted + no majority of D bits inverted
dec_req	majority of D bits inverted + no majority of I bits inverted

Notes

1. The active offset is defined as the accepted current phase of the SPE (VC) in the NORM_state and is undefined in the other states.
2. Enabled NDF is defined as the following bit patterns: 1001, 0001, 1101, 1011, 1000.
3. Disabled NDF is defined as the following bit patterns: 0110, 1110, 0010, 0100, 0111.
4. The remaining six NDF codes (0000, 0011, 0101, 1010, 1100, 1111) result in an inv_ndf indication.
5. The ss bits are unspecified in SONET and have bit pattern 10 in SDH
6. The use of ss bits in definition of indications may be optionally disabled.
7. The requirement for a previous NDF_enable, inc_ind or dec_ind be more than 3 frames ago may be optionally disabled.
8. New_point is also an inv_point.
9. LOP is not declared if all the following conditions exist:
   - the received pointer is out of range (>782),
   - the received pointer is static,
   - the received pointer can be interpreted, according to majority voting on the I and D bits, as a positive or negative justification indication,
   - after making the requested justification, the received pointer continues to be interpretable as a pointer justification.

   When the received pointer returns to an in-range value, the S/UNI-1x155 will interpret it correctly.
10. LOP will exit at the third frame of a three frame sequence consisting of one frame with NDF enabled followed by two frames with NDF disabled, if all three pointers have the same legal value.
11. For the purposes of 8xNDF_enable only, the requirement of the pointer to be within the range of 0 to 782 may be optionally disabled.

The transitions indicated in the state diagram are defined in the following table.

Table 3 Pointer Interpreter Transition Description

Transition	Description
inc_ind/dec_ind	offset adjustment (increment or decrement indication)
3 x eq_new_point	three consecutive equal new_point indications
NDF_enable	single NDF_enable indication
3 x AIS_ind	three consecutive AIS indications
8 x inv_point	eight consecutive inv_point indications
8 x NDF_enable	eight consecutive NDF_enable indications

Notes

1. The transitions from NORM_state to NORM_state do not represent state changes but imply offset changes.
2. 3 x new_point takes precedence over other events and if the IINVCNT bit is set resets the inv_point count.
3. All three offset values received in 3 x eq_new_point must be identical.
4. The "consecutive event counters" are reset to zero on a change of state except for consecutive NDF count.

The Pointer Interpreter detects loss of pointer (LOP) in the incoming STS-3c/STM-1 stream. LOP is declared on entry to the LOP_state as a result of eight consecutive invalid pointers or eight consecutive NDF enabled indications. The alarm condition is reported in the receive alarm port and is optionally returned to the source node by signaling the corresponding Transmit Path Overhead Processor in the local S/UNI-1x155 to insert a path RDI indication.

The Pointer Interpreter detects path AIS in the incoming STS-3c/STM-1 stream. PAIS is declared on entry to the AIS_state after three consecutive AIS indications. The alarm condition is reported in the receive alarm port and is optionally returned to the source node by signaling the corresponding Transmit Path Overhead Processor in the local SONET/SDH equipment to insert a path RDI indication.

Invalid pointer indications (inv_point), invalid NDF codes, new pointer indications (new_point), discontinuous change of pointer alignment, and illegal pointer changes are also detected and reported by the Pointer Interpreter block via register bits. An invalid NDF code is any NDF code that does not match the NDF enabled or NDF disabled definitions. The third occurrence of equal new_point indications (3 x eq_new_point) is reported as a discontinuous change of pointer alignment event (DISCOPA) instead of a new pointer event and the active offset is updated with the receive pointer value. An illegal pointer change is defined as a inc_ind or dec_ind indication that occurs within three frames of the previous inc_ind, dec_ind or NDF_enable indications. Illegal pointer changes may be optionally disabled via register bits.

The active offset value is used to extract the path overhead from the incoming stream and can be read from an internal register.

10.6.2 SPE Timing

The SPE Timing Block provides SPE timing information to the Error Monitor and the Extract blocks. The block contains a free running timeslot counter that is initialized by a J1 byte identifier (which identifies the first byte of the SPE). Control signals are provided to the Error Monitor and the Extract blocks to identify the Path Overhead bytes and to downstream circuitry to extract the ATM cell or POS payload.

10.6.3 Error Monitor

The Error Monitor Block contains two 16-bit counters that are used to accumulate path BIP-8 errors (B3), and far end block errors (FEBEs). The contents of the two counters may be transferred to holding registers, and the counters reset under microprocessor control.

Path BIP-8 errors are detected by comparing the path BIP-8 byte (B3) extracted from the current frame, to the path BIP-8 computed for the previous frame.

FEBEs are detected by extracting the 4-bit FEBE field from the path status byte (G1). The legal range for the 4-bit field is between 0000 and 1000, representing zero to eight errors. Any other value is interpreted as zero errors.

Path RDI alarm is detected by extracting bit 5 of the path status byte. The PRDI signal is set high when bit 5 is set high for five/ten consecutive frames. PRDI is set low when bit 5 is low for five/ten consecutive frames. Auxiliary RDI alarm is detected by extracting bit 6 of the path status byte. The Auxiliary RDI alarm is indicated when bit 6 is set high for five/ten consecutive frames. The Auxiliary RDI alarm is removed when bit 6 is low for five/ten consecutive frames. The Enhanced RDI alarm is detected when the enhanced RDI code in bits 5,6,7 of the path status byte indicates the same error codepoint for five/ten consecutive frames. The Enhanced RDI alarm is removed when the enhanced RDI code in bits 5,6,7 of the path status byte indicates the same non error codepoint for five/ten consecutive frames. The ERDII maskable interrupt is set high when bits 5, 6 & 7 of the path status byte (G1) byte are set to a new codepoint for five or ten consecutive frames. The ERDIV[2:0] signal reflects the state of the filtered ERDI value (G1 byte bits 5, 6, & 7).

10.7 Receive Path Overhead Extract

The Path Overhead Extract Block extracts and serializes the receive path overhead bytes on RPOH. Output RPOHFP is provided to identify the most significant bit of the path trace byte (J1) on RPOH. The path overhead clock, RPOHCLK is nominally a 576 kHz clock. RPOH and RPOHFP are updated on the falling edge of RPOHCLK.

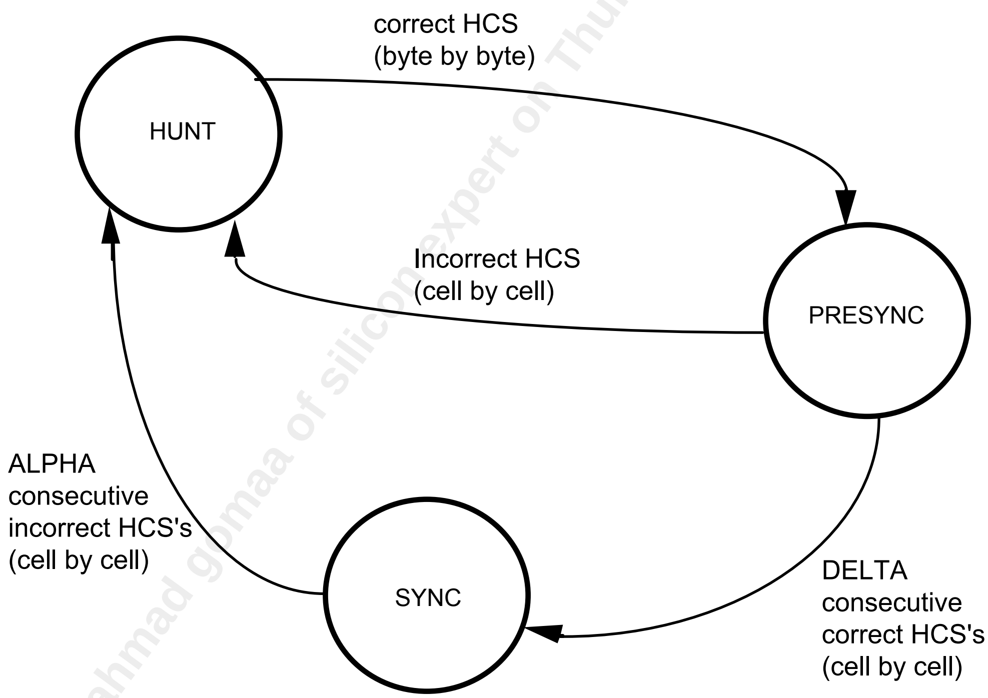
10.8 Receive ATM Cell Processor (RXCP)

The Receive ATM Cell Processor (RXCP) performs ATM cell delineation, provides cell filtering based on idle/unassigned cell detection and HCS error detection, and performs ATM cell payload descrambling.

10.8.1 Cell Delineation

Cell Delineation is the process of framing to ATM cell boundaries using the header check sequence (HCS) field found in the cell header. The HCS is a CRC-8 calculation over the first 4 octets of the ATM cell header. When performing delineation, correct HCS calculations are assumed to indicate cell boundaries. Cells are assumed to be byte-aligned to the synchronous payload envelope. The cell delineation algorithm searches the 53 possible cell boundary candidates individually to determine the valid cell boundary location. While searching for the cell boundary location, the cell delineation circuit is in the HUNT state. When a correct HCS is found, the cell delineation state machine locks on the particular cell boundary, corresponding to the correct HCS, and enters the PRESYNC state. The PRESYNC state validates the cell boundary location. If the cell boundary is invalid, an incorrect HCS will be received within the next DELTA cells, at which time a transition back to the HUNT state is executed. If no HCS errors are detected in this PRESYNC period, the SYNC state is entered. While in the SYNC state, synchronization is maintained until ALPHA consecutive incorrect HCS patterns are detected. In such an event a transition is made back to the HUNT state. The state diagram of the delineation process is shown in Figure 5.

Figure 5 Cell Delineation State Diagram



The values of ALPHA and DELTA determine the robustness of the delineation process. ALPHA determines the robustness against false misalignments due to bit errors. DELTA determines the robustness against false delineation in the synchronization process. ALPHA is chosen to be 7 and DELTA is chosen to be 6. These values result in an average time to delineation of 32 µs for the STS-3c/STM-1 rate.

10.8.2 Descrambler

The self-synchronous descrambler operates on the 48 byte cell payload only. The circuitry descrambles the information field using the $x^{43} + 1$ polynomial. The descrambler is disabled for the duration of the header and HCS fields and may optionally be disabled for the payload.

10.8.3 Cell Filter and HCS Verification

Cells are filtered (or dropped) based on HCS errors and/or a cell header pattern. Cell filtering is optional and is enabled through the RXCP registers. Cells are passed to the receive FIFO while the cell delineation state machine is in the SYNC state as described above. When both filtering and HCS checking are enabled, cells are dropped if uncorrectable HCS errors are detected, or if the corrected header contents match the pattern contained in the RXCP Match Header Pattern and RXCP Match Header Mask registers. Idle or unassigned cell filtering is accomplished by writing the appropriate cell header pattern into the RXCP Match Header Pattern and RXCP Match Header Mask registers. Idle/Unassigned cells are assumed to contain the all zeros pattern in the VCI and VPI fields. The RXCP Match Header Pattern and RXCP Match Header Mask registers allow filtering control over the contents of the GFC, PTI, and CLP fields of the header.

The HCS is a CRC-8 calculation over the first 4 octets of the ATM cell header. The RXCP block verifies the received HCS using the polynomial, $x^8 + x^2 + x + 1$. The coset polynomial, $x^6 + x^4 + x^2 + 1$, is added (modulo 2) to the received HCS octet before comparison with the calculated result.

10.8.4 Performance Monitor

The Performance Monitor consists of two 8-bit saturating HCS error event counters and a 24-bit saturating receive cell counter. The 24-bit receive cell counter counts all cells written into the receive FIFO. Filtered cells are not counted.

Each counter may be read through the microprocessor interface. Circuitry is provided to latch these counters so that their values can be read while simultaneously resetting the internal counters to 0 or 1, if appropriate, so that a new period of accumulation can begin without loss of any events. It is intended that the counter be polled at least once per second so as not to miss any counted events.

10.9 Receive POS Frame Processor (RXFP)

The Receive POS Frame Processor (RXFP) performs packet extraction, provides FCS error correction, performs packet payload descrambling, and provides performance monitoring functions.

10.9.1 Overhead Removal

The overhead removal consists of stripping SONET/SDH overhead bytes from the data stream. Once overhead bytes are removed, the data stream consists of POS frame octets that can be fed directly to the descrambler or the POS Frame Delineation block.

10.9.2 Descrambler

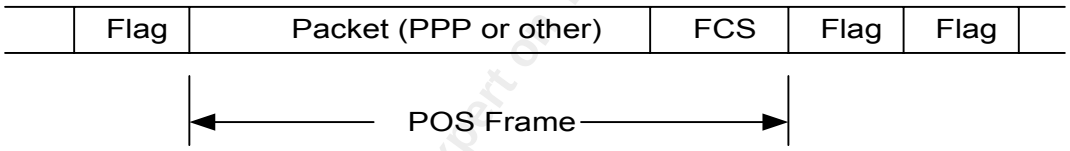
When enabled, the self-synchronous descrambler operates on the POS Frame data, descrambling the data with the polynomial $x^{43} + 1$. Descrambling is performed on the raw data stream, before any POS frame delineation or byte destuffing is performed. Data scrambling can provide for a more robust system, preventing the injection of hostile patterns into the data stream.

10.9.3 POS Frame Delineation

This block accepts data one byte at a time and arranges it as POS framed octets. Frame boundaries are found by searching for the Flag Character (0x7E). Flags are also used to fill inter-packet spacing. This block removes the Flag Sequence and passes the data onto the Byte Destuffing block.

The POS Frame Delineation is performed on the descrambled data and consists of arranging the POS framed octets. Frame boundaries are found by searching for the Flag Character (0x7E). Flags are also used to fill inter-packet spacing. This block removes the Flag Sequence and passes the data onto the Byte Destuffing block. The POS Frame format is shown on Figure 6.

Figure 6 Packet Over SONET/SDH Frame Format



In the event of a FIFO overflow caused by the FIFO being full while a packet is being received, the packet is marked with an error so it can be discarded by the system. Subsequent bytes associated with this now aborted frame are discarded. Reception of POS data resumes when a Start of Packet is encountered and the FIFO level is below the programmable Reception Initialization Level (RIL[7:0]).

10.9.4 Byte Destuffing

The byte destuffing algorithm searches the Control Escape character (0x7D). These characters, listed in Table 4, are added for transparency in the transmit direction and must be removed to recover the user data. When the Control Escape character is encountered, it is removed and the following data byte is XORed with 0x20. Therefore, any escaped data byte will be processed properly by the S/UNI-1x155.

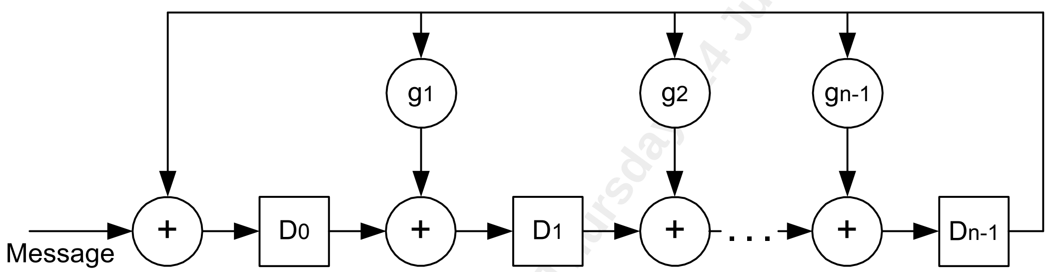
Table 4 HDLC Byte Sequences

Data Value	Sequence
0x7E (Flag Sequence)	0x7D 0x5E
0x7D (Control Escape)	0x7D 0x5D
HDLC Aborted Packet	0x7D 0x7E

10.9.5 FCS Check

The FCS Generator performs a CRC-16.ISO-3309 or CRC-32 calculation on the whole POS frame, after byte destuffing and data descrambling scrambling. A parallel implementation of the CRC polynomial is used. The CRC algorithm for the frame checking sequence (FCS) field is either a CRC-16.ISO-3309 or CRC-32 function. The CRC-16.ISO-3309 is two bytes in size and has a generating polynomial $g(x) = 1 + x^5 + x^{12} + x^{16}$. The CRC-32 is four bytes in size and has a generating polynomial $g(x) = 1 + x + x^2 + x^4 + x^5 + x^7 + x^8 + x^{10} + x^{11} + x^{12} + x^{16} + x^{22} + x^{23} + x^{26} + x^{32}$. The first FCS bit transmitted is the coefficient of the highest term. Packets with FCS errors are marked as such and should be discarded by the system.

Figure 7 CRC Decoder



10.9.6 Performance Monitor

The Performance Monitor consists of four 16-bit saturating error event counters and one 24-bit saturating received good packet counter. One of the error event counters accumulates FCS errors. The second error event counter accumulates minimum length violation packets. The third error event counter accumulates maximum length violation packets. The fourth error event counter accumulates aborted packets. The 24-bit receive good packet counter counts all error free packets.

Each counter may be read through the microprocessor interface. Circuitry is provided to latch these counters so that their values can be read while simultaneously resetting the internal counters to 0 or 1, whichever is appropriate, so that a new period of accumulation can begin without loss of any events. The counters should be polled at least once per second so error events will not be missed.

The RXFP monitors the packets for both minimum and maximum length errors. When a packet size is smaller than MINPL[7:0], the packet is marked with an error but still written into the FIFO. Malformed packets, that is packets that do not at least contain the FCS field plus one byte, are treated differently. If a malformed packet is received and FCS stripping is enabled, the packet is discarded, not written in the FIFO, and counted as a minimum packet size violation. If a malformed packet is received and FCS stripping is disabled, it is written into the FIFO since, in this case, the misformed packet criteria is reduced to one byte, but will still count as a minimum packet size violation. When the packet size exceeds MAXPL[15:0] the packet is marked with an error and the bytes beyond the maximum count are discarded.

Receive FIFO management functions include filling the receive FIFO, indicating when packets or bytes are available to be read from the receive FIFO, maintaining the receive FIFO read and write pointers, and detecting FIFO overrun and underrun conditions. Upon detection of an overrun, the FIFO aborts the current packet and discards the current incoming bytes until there is room in the FIFO. Once enough room is available, as defined by the RIL[7:0] register, the RXFP will wait for the next start of packet before writing any data into the FIFO. FIFO overruns are indicated through a maskable interrupt and register bit, and are considered a system error. A FIFO underrun is caused when the System Interface tries to read more data words while the FIFO is empty. This action will be detected and reported through the FUDRI interrupt, but it is not considered a system error. The system will continue to operate normally. In that situation, RVAL can be used by the Link Layer device to find out if valid or invalid data is provided on the System Interface.

10.10 Transmit Line Interface (CSPI)

The Transmit Line Interface allows to directly interface the S/UNI-1x155 with optical modules (ODLs) or other medium interfaces. This block performs clock synthesis and performs parallel to serial conversion on each outgoing 155.52 Mbit/s data stream.

10.10.1 Clock Synthesis

The transmit clock is synthesized from a 19.44 MHz reference by the clock synthesis unit (CSU). The transfer function yields a typical low pass corner of 1 MHz, above which reference jitter is attenuated at least 20 dB per octave. The design of the loop filter and PLL is optimized for minimum intrinsic jitter. With a jitter free 19.44 MHz reference, the intrinsic jitter is typically less than 0.006 UI RMS when measured using a high pass filter with a 12 kHz cutoff frequency. The REFCLK reference should be within ±20 ppm to meet the SONET/SDH free-run accuracy requirements specified in GR-253-CORE.

10.10.2 Parallel to Serial Converter

The Parallel to Serial Converter (PISO) converts each transmit byte serial stream to a bit serial stream. The transmit bit serial streams appear on the TXD+/- PECL outputs.

10.11 Transmit Section Overhead Processor (TSOP)

The Transmit Section Overhead Processor (TSOP) provides frame pattern insertion (A1, A2), scrambling, section level alarm signal insertion, and section BIP-8 (B1) insertion. In addition, it may insert the section data communication channel provided serially on the transmit DCC inputs.

10.11.1 Line AIS Insert

Line AIS insertion results in all bits of the SONET/SDH frame being set to 1 before scrambling except for the section overhead. The Line AIS Insert Block substitutes all ones as described when enabled by the TLAIS input or through an internal register accessed through the microprocessor interface. Activation or deactivation of line AIS insertion is synchronized to frame boundaries.

10.11.2 Data Link Insert

The Data Link Insert Block inserts the section data communication channel (bytes D1, D2, and D3) into the STS-3c/STM-1 stream when enabled by an internal register accessed via the common bus interface. The bytes to be inserted are serially input on the associated TDCC signal at a nominal 192 kbit/s rate. Timing for upstream processing of the data communication channel is provided by the TDCLK signal. TDCLK is derived from a 216 kHz clock that is gapped to yield an average frequency of 192 kHz.

10.11.3 BIP-8 Insert

The BIP-8 Insert Block calculates and inserts the BIP-8 error detection code (B1) into the transmit stream.

The BIP-8 calculation is based on the scrambled data of the complete STS-3c/STM-1 frame. The section BIP-8 code is based on a bit interleaved parity calculation using even parity. Details are provided in the references. The calculated BIP-8 code is then inserted into the B1 byte of the following frame before scrambling. BIP-8 errors may be continuously inserted under register control for diagnostic purposes.

10.11.4 Framing and Identity Insert

The Framing and Identity Insert Block inserts the framing bytes (A1, A2) and trace/growth bytes (J0/Z0) into the STS-3c/STM-1 frame. Framing bit errors may be continuously inserted under register control for diagnostic purposes.

10.11.5 Scrambler

The Scrambler Block utilizes a frame synchronous scrambler to process the transmit stream when enabled through an internal register accessed via the microprocessor interface. The generating polynomial is $x^7 + x^6 + 1$. Precise details of the scrambling operation are provided in the references. Note that the framing bytes and the identity bytes are not scrambled. All zeros may be continuously inserted (after scrambling) under register control for diagnostic purposes.

10.12 Transmit Line Overhead Processor (TLOP)

The Transmit Line Overhead Processor (TLOP) provides line level alarm signal insertion, and line BIP-24 insertion (B2). In addition, it inserts the line data communication provided serially on the transmit DCC inputs.

10.12.1 APS Insert

The APS Insert Block inserts the two automatic protection switch (APS) channel bytes in the Line Overhead (K1 and K2) into the transmit stream when enabled by an internal register.

10.12.2 Data Link Insert

The Data Link Insert Block inserts the line data communication channel (DCC) (bytes D4 to D12) into the STS-3c/STM-1 stream when enabled by an internal register. The D4 to D12 bytes are input serially using the associated TDCC signal at a nominal 576 kbit/s rate. Timing for upstream processing of the line DCC is provided by the TDCLK output. TDCLK is derived from a 2.16 MHz clock that is gapped to yield an average frequency of 576 kHz.

10.12.3 Line BIP Calculate

The Line BIP Calculate Block calculates the line BIP-24 error detection code (B2) based on the line overhead and synchronous payload envelope of the transmit stream. The line BIP-24 code is a bit interleaved parity calculation using even parity. Details are provided in the references. The calculated BIP-24 code is inserted into the B2 byte positions of the following frame. BIP-24 errors may be continuously inserted under register control for diagnostic purposes.

10.12.4 Line RDI Insert

The Line RDI Insert Block controls the insertion of line remote defect indication. Line RDI insertion is enabled through register control. Line RDI is inserted by transmitting the code 110 (binary) in bit positions 6, 7, and 8 of the K2 byte contained in the transmit stream.

10.12.5 Line FEBE Insert

The Line FEBE Insert Block accumulates line BIP-24 errors (B2) detected by the Receive Line Overhead Processor and encodes far end block error indications in the transmit Z2 byte.

10.13 Transmit Power Supply Filter Overhead Insert Port

The Transport Overhead Insert Port allows the complete transport overhead to be inserted using input TTOH, along with the transport overhead clock, TTOHCLK, and the transport overhead frame position, TTOHFP. The transport overhead clock, TTOHCLK, is nominally a 5.184 MHz clock. The transport overhead enable signal, TTOHEN, controls the insertion of transport overhead from TTOH.

The state of the TTOHEN input determines whether the data sampled on TTOH, or the default overhead byte values are inserted in the transmit stream. For example, a high level on TTOHEN during the section user channel (F1) bit positions causes the eight values shifted in the TTOH input to be inserted in the F1 byte position in the transmit stream. A low level on TTOHEN during the section user channel bit positions causes the default value to be inserted in the transmit stream.

10.14 Transmit Path Overhead Processor (TPOP)

The Transmit Path Overhead Processor (TPOP) provides transport frame alignment generation, pointer generation (H1, H2), path overhead insertion and the insertion of path level alarm signals.

10.14.1 Pointer Generator

The Pointer Generator Block generates the outgoing payload pointer (H1, H2) as specified in the references. The concatenation indication (the NDF field set to 1001, I-bits and D-bits set to all ones, and unused bits set to all zeros) is inserted in the second and third pointer byte locations in the transmit stream.

(1) A "normal pointer value" locates the start of the SPE. Note: 0 ≤ "normal pointer value" ≤ 782, and the new data flag (NDF) field is set to 0110. Note that values greater than 782 may be inserted, using internal registers, to generate a loss of pointer alarm in downstream circuitry.

(2) Arbitrary "pointer values" may be generated using internal registers. These new values may optionally be accompanied by a programmable new data flag. New data flags may also be generated independently using internal registers.

(3) Positive pointer movements may be generated using a bit in an internal register. A positive pointer movement is generated by inverting the five I-bits of the pointer word. The SPE is not inserted during the positive stuff opportunity byte position, and the pointer value is incremented by one. Positive pointer movements may be inserted once per frame for diagnostic purposes.

(4) Negative pointer movements may be generated using a bit in an internal register. A negative pointer movement is generated by inverting the five D-bits of the pointer word. The SPE is inserted during the negative stuff opportunity byte position, the H3 byte, and the pointer value is decremented by one. Negative pointer movements may be inserted once per frame for diagnostic purposes.

The pointer value is used to insert the path overhead into the transmit stream. The current pointer value may be read via internal registers.

10.14.2 BIP-8 Calculate

The BIP-8 Calculate Block performs a path bit interleaved parity calculation on the SPE of the transmit stream. Details are provided in the references. The resulting parity byte is inserted in the path BIP-8 (B3) byte position of the subsequent frame. BIP-8 errors may be continuously inserted under register control for diagnostic purposes.

10.14.3 FEBE Calculate

The FEBE Calculate Block accumulates far end block errors on a per frame basis, and inserts the accumulated value (up to maximum value of eight) in the FEBE bit positions of the path status (G1) byte. The FEBE information is derived from path BIP-8 errors detected by the receive path overhead processor, RPOP. Far end block errors may be inserted under register control for diagnostic purposes.

10.15 Transmit Path Overhead Insert

The Path Overhead Insert Port allows the complete path overhead to be inserted using input TPOH, along with the path overhead clock, TPOHCLK, and the path overhead frame position, TPOHFP. The path overhead clock, TPOHCLK, is nominally a 576 kHz clock. The state of the TPOHEN input, together with an internal register, determines whether the data sampled on TPOH, or the default path overhead byte values are inserted in the transmit stream. For example, a high level on TPOHEN during the path signal label (C2) bit positions causes the eight values shifted in on TPOH to be inserted in the C2 byte position in the transmit stream. A low level on TPOHEN during the path signal label bit positions causes the provisioned value to be inserted in the transmit stream.

During the B3 byte position in the TPOH stream, a high level on TPOHEN enables an error insertion mask. While the error mask is enabled, a high level on input TPOH causes the corresponding bit in the B3 byte to be inverted. A low level on TPOH causes the corresponding bit in the B3 byte to be transmitted uncorrupted.

10.16 Transmit ATM Cell Processor (TXCP)

The Transmit ATM Cell Processor (TXCP) provides rate adaptation via idle/unassigned cell insertion, provides HCS generation and insertion, and performs ATM cell scrambling. An idle or unassigned cell is transmitted if a complete ATM cell has not been written into the transmit FIFO.

10.16.1 Idle/Unassigned Cell Generator

The Idle/Unassigned Cell Generator inserts idle or unassigned cells into the cell stream when enabled. Registers are provided to program the GFC, PTI, and CLP fields of the idle cell header and the idle cell payload. The idle cell HCS is automatically calculated and inserted.

10.16.2 Scrambler

The Scrambler scrambles the 48 octet information field. Scrambling is performed using a parallel implementation of the self-synchronous scrambler ($x^{43} + 1$ polynomial). The cell headers are transmitted unscrambled, and the scrambler may optionally be disabled.

10.16.3 HCS Generator

The HCS Generator performs a CRC-8 calculation over the first four header octets. A parallel implementation of the polynomial, x^8+x^2+x+1, is used. The coset polynomial, $x^6+x^4+x^2+1$, is added (modulo 2) to the residue. The HCS Generator optionally inserts the result into the fifth octet of the header.

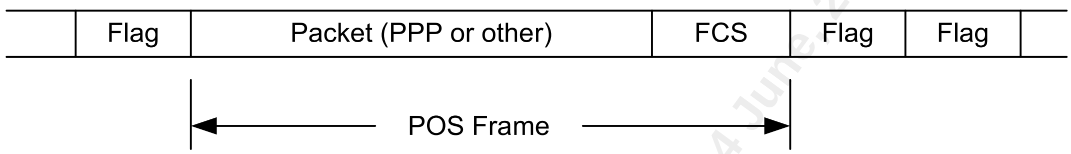
10.17 Transmit POS Frame Processor (TXFP)

The Transmit POS Frame Processor (TXFP) provides rate adaptation by transmitting flag sequences (0x7E) between packets, provides FCS generation and insertion, performs packet data scrambling, and provides performance monitoring functions.

10.17.1 POS Frame Generator

The POS Frame Generator runs off of the SONET/SDH sequencer to create the POS frames to be transmitted, whose format is shown in Figure 8. Flags are inserted whenever the Transmit FIFO is empty and there is no data to transmit. When there is enough data to be transmitted, the block operates normally; it removes packets from the Transmit FIFO and transmits them. In addition, FCS generation, error insertion, byte stuffing, and scrambling can be optionally enabled.

Figure 8 Packet Over SONET/SDH Frame Format



In the event of a FIFO underflow caused by the FIFO being empty while a packet is being transmitted, the packet is aborted by transmitting the Abort Sequence. The Abort Sequence consists of an Escape Control character (0x7D) followed by the Flag Sequence (0x7E). Bytes associated with this aborted frame are still read from the FIFO but are discarded and replaced with the Flag Sequence in the outgoing data stream. Transmission of data resumes when the start of the next packet is encountered in the FIFO data stream.

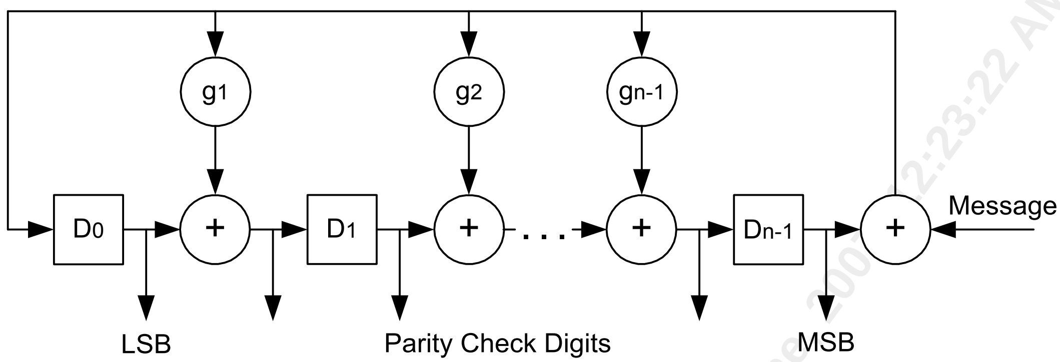
The POS Frame Generator also performs inter-packet gaping. This operation consists of inserting a programmable number of Flag Sequence characters between each POS frame transmission. This feature allows control of the system's effective data transmission rate if required.

For correct operation, the TXFP only supports packets ranging in size from 2 bytes to 65534 bytes in length.

10.17.2 FCS Generator

The FCS Generator performs a CRC-16.ISO-3309 or CRC-32 calculation on the whole POS frame, before byte stuffing and data scrambling. A parallel implementation of the CRC polynomial is used. The CRC algorithm for the frame checking sequence (FCS) field is either a CRC-16.ISO-3309 or CRC-32 function. The CRC-16.ISO-3309 is two bytes in size and has a generating polynomial $g(x) = 1 + x^5 + x^{12} + x^{16}$. The CRC-32 is four bytes in size and has a generating polynomial $g(x) = 1 + x + x^2 + x^4 + x^5 + x^7 + x^8 + x^{10} + x^{11} + x^{12} + x^{16} + x^{22} + x^{23} + x^{26} + x^{32}$. The first FCS bit transmitted is the coefficient of the highest term. When transmitting a packet from the Transmit FIFO, the FCS Generator appends the result after the last data byte, before the closing flag. Note that the Frame Check Sequence is the one's complement of the CRC register after calculation ends. FCS calculation and insertion can be disabled.

Figure 9 CRC Generator



An error insertion mechanism is provided for system diagnosis purposes. Error insertion is performed by inverting the resulting FCS value, before transmission. This should cause an FCS Error at the far end.

10.17.3 Byte Stuffing

The POS Frame generator provides transparency by performing byte stuffing. This operation is done after the FCS calculation. Two characters are being escaped, the Flag Sequence (0x7E) and the Escape Character itself (0x7D). When a character is being escaped, it is XORed with 0x20 before transmission and preceded by the Control Escape (0x7D) character.

Table 5 HDLC Byte Sequences

Data Value	Sequence
0x7E (Flag Sequence)	0x7D 0x5E
0x7D (Control Escape)	0x7D 0x5D
HDLC Abort Sequence	0x7D 0x7E

10.17.4 Data Scrambling

The Scrambler will optionally scramble the whole packet data, including the FCS and the flags. Scrambling is performed after the POS frame is formed using a parallel implementation of the self-synchronous scrambler polynomial, $x^{43}+1$. On reset, the scrambler is set to all ones to ensure scrambling on start-up. The scrambler may optionally be completely disabled. Data scrambling can provide for a more robust system preventing the injection of hostile patterns into the data stream.

10.17.5 SONET/SDH Framer

The SONET/SDH Framer gaps the POS frames in order to insert the SONET/SDH framing and overhead bytes (Section/Line Overhead and Path Overhead). The framer uses framing alignment information provided by the TPOP TSB to perform its function. The TXFP does not set any SONET/SDH overhead bytes.

10.18 SONET/SDH Path Trace Buffer (SPTB)

The SONET/SDH Section Trace Buffer (SPTB) block can handle both 64-byte CLLI messages in SONET and 16-byte E.164 messages in SDH. This block operates similarly to the SONET/SDH Section Trace Buffer (SSTB) except the C2 byte is also processed.

10.18.1 Receive Trace Message Receiver

When TIMODE is low, the Trace Message Receiver (TMR) captures the received path trace identifier message (J1 byte) into microprocessor readable register. It contains three pages of trace message memory. They are the capture page, the accepted page and the expected page. Path trace identifier data bytes from the receive stream are written into the capture page. The expected identifier message is written by the microprocessor into the expected page.

On receipt of a trace identifier byte, it is written into the next location in the capture page. The received byte is compared with the data from the previous message in the capture page. An identifier message is accepted if it is received unchanged three times or, optionally, five times. The accepted message is then compared with the expected message. If the current message differs from the previous message for eight consecutive messages, the received message is declared unstable. The received message is declared stable when the received message passes the persistency criterion (three or five identical receptions) for being accepted. An interrupt may be optionally generated on entry to and exit from the unstable state.

The length of the path trace identifier message is selectable between 16 bytes and 64 bytes. When programmed for 16 byte messages, the path trace buffer synchronizes to the byte with the most significant bit set to high and places the byte at the first location in the capture page. When programmed for 64 byte messages, the path trace buffer synchronizes to the trailing carriage return (CR = 0DH), line feed (LF = 0AH) sequence and places the next byte at the head of the capture page. This enables the path trace message to be appropriately aligned for interpretation by the microprocessor. Synchronization may be disabled, in which case the memory acts as a circular buffer.

When TIMODE is high, a stable message is declared when forty eight of the same path trace identifier message (J1) bytes are received. Once in the stable state, an unstable state is declared when one or more errors are detected in three consecutive sixteen byte windows.

10.18.2 Transmit Trace Buffer

The Trace Transmit Buffer (TTB) sources the 16-byte or 64-byte trace identifier message. The TTB contains one page of transmit trace identifier message memory. Identifier message data bytes are written by the microprocessor into the message buffer and inserted in the transmit stream. When the microprocessor is updating the transmit page buffer, the TTB may be programmed to transmit null characters to prevent transmission of partial messages.

10.18.3 Overhead Byte Receiver

The path signal label (PSL) found in the path overhead byte (C2) is processed. Two detection algorithms are implemented for the declaration of path signal label mismatch.

When PSLMODE is low, an incoming PSL is accepted when it is received unchanged for five consecutive frames. The accepted PSL is compared with the provisioned value. The PSL alarm declarations are determined by Table 6.

Each time an incoming PSL differs from the one in the previous frame, the PSL unstable counter is incremented. Thus, a single bit error in the PSL in a sequence of constant PSL values will cause the counter to increment twice, once on the errored PSL and again on the first error-free PSL. The incoming PSL is considered unstable when the counter reaches five. The counter is cleared when the same PSL is received for five consecutive frames.

Table 6 Path Signal Label Mismatch Mechanism

Expect	Receive	Action
00	00	Match
00	01	Mismatch
00	XX	Mismatch
01	00	Mismatch
01	01	Match
01	XX	Match
XX	00	Mismatch
XX	01	Match
XX	XX	Match
XX	YY	Mismatch

Note

- XX, YY are equal to anything except 0x00 or 0x01 and are not equal to each other.

When PSLMODE is high, the receive path signal mismatch alarm is declared based on the declaration of a match or mismatch between the received label and the expected label. The mismatch is set when five consecutive mismatches are declared. The mismatch is cleared when five consecutive matches are declared. Table 7 shows the alarm declarations determined by the different received and expected labels.

Table 7 Path Signal Label Mismatch Mechanism

Expect	Receive	Action
00	00	Unequipped
00	01	Mismatch
00	XX	Mismatch
01	00	Unequipped
01	01	Match
01	XX	Match
XX	00	Unequipped
XX	01	Match
XX	XX	Match
XX	YY	Mismatch

Note

- XX, YY are equal to anything except 0x00 or 0x01 and are not equal to each other.

10.19 SONET/SDH Section Trace Buffer (SSTB)

The SONET/SDH Section Trace Buffer (SSTB) block can handle both 64-byte CLLI messages in SONET and 16-byte E.164 messages in SDH. This block operates similarly to the SONET/SDH Path Trace Buffer (SPTB).

10.19.1 Receive Trace Message Receiver

When TIMODE is low, the Trace Message Receiver (TMR) captures the received section trace identifier message (J0 byte) into microprocessor readable register. It contains three pages of trace message memory. They are the capture page, the accepted page and the expected page. Section trace identifier data bytes from the receive stream are written into the capture page. The expected identifier message is written by the microprocessor into the expected page.

On receipt of a trace identifier byte, it is written into next location in the capture page. The received byte is compared with the data from the previous message in the capture page. An identifier message is accepted if it is received unchanged three times or, optionally, five times. The accepted message is then compared with the expected message. If the current message differs from the previous message for eight consecutive messages, the received message is declared unstable. The received message is declared stable when the received message passes the persistency criterion (three or five identical receptions) for being accepted. An interrupt may be optionally generated on entry to and exit from the unstable state.

The length of the section trace identifier message is selectable between 16 bytes and 64 bytes. When programmed for 16 byte messages, the section trace buffer synchronizes to the byte with the most significant bit set to high and places the byte at the first location in the capture page. When programmed for 64 byte messages, the section trace buffer synchronizes to the trailing carriage return (CR = 0DH), line feed (LF = 0AH) sequence and places the next byte at the head of the capture page. This enables the section trace message to be appropriately aligned for interpretation by the microprocessor. Synchronization may be disabled, in which case, the memory acts as a circular buffer.

When TIMODE is high, a stable message is declared when forty eight of the same section trace identifier message (J0) bytes are received. Once in the stable state, an unstable state is declared when one or more errors are detected in three consecutive sixteen byte windows.

10.19.2 Transmit Trace Buffer (TTB)

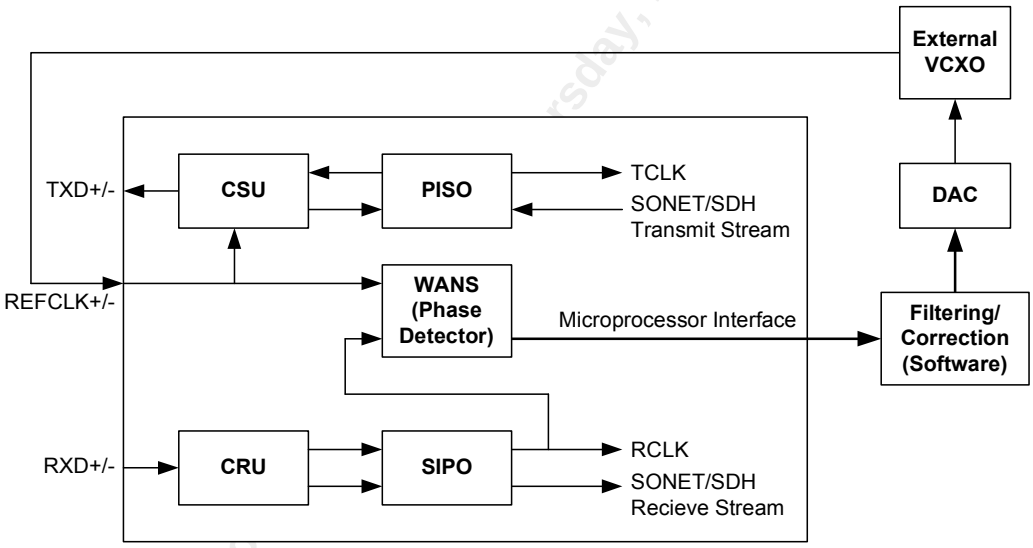
The TTB sources the 16-byte or 64-byte trace identifier message. The TTB contains one page of transmit trace identifier message memory. Identifier message data bytes are written by the microprocessor into the message buffer and inserted in the transmit stream. When the microprocessor is updating the transmit page buffer, the TTB may be programmed to transmit null characters to prevent transmission of partial messages.

10.20 WAN Synchronization Controller (WANS)

The WANS provides hardware support to implement a local clock reference compliant to SONET/SDH Stratum 3 clock specifications (GR-253-CORE & GR-1244-CORE) in wander transfer, long term and holdover stability. The WANS block is intended to be used in conjunction with an external processor, digital to analog converter (DAC), analog circuitry and voltage control crystal oscillator (VCXO).

In general, WANS block implements the phase detector of a phase lock loop structure which relies on an external processor and a VCXO to produce the Stratum 3 clock as shown in Figure 10. The WANS performs a digital phase comparison between the recovered receive clock (receive line rate clock from a clock recovery unit) and the reference clock used to generate the transmit stream (REFCLK supplied by the VCXO).

Figure 10 WANS PLL Block Diagram



The software running on the external processor is responsible for performing: digital loop filtering, temperature compensation, VCXO linearity compensation; determining the validity of the timing reference; and performing reference switchover. The VCXO creates the 19.44 MHz Stratum 3 reference clock which the CSU will synthesize to the desired 155.52 MHz transmit clock.

Thus, the WANS PLL structure can phase lock the SONET/SDH transmit serial stream to the SONET/SDH receive serial stream. With appropriate software filtering and compensation, the device may meet SONET/SDH Stratum 3 clock specifications (GR-253-CORE & GR-1244-CORE) in wander transfer, long term and holdover stability.

A description of how to program and use the WANS feature can be found in the TETRA reference design (PMC-1980322).

A description of the functionality supplied by the WANS block is given below.

10.20.1 Phase Comparison

The phase comparison between the receive recovered clock (RCLK) and the transmit reference clock (REFCLK) is implemented by sampling, at a fixed interval specified by the Reference Counter, the output of the Phase Counter. The Reference Counter is clocked by RCLK while the Phase Counter is clocked by the REFCLK clock.

Successive reading of the value obtained, referred as the phase sample (PHSAMP), can be used to calculate the phase relation between both clocks. Both the Reference Counter and the Phase Counter are programmable counters and are set to have equal cycle period. Therefore, if REFCLK was phased locked to RCLK, successive readings of the phase sample would be equal. The phase sample value will increase or decrease depending if REFCLK is faster or slower than RCLK.

At each reference period, a signal enabling the sampling (SAMPLEN) of the Phase Counter is produced. This signal is resynchronized to REFCLK to avoid any potential metastability problem that could result due to the asynchronous nature of both clocks.

10.20.2 Phase Reacquisition Control

The Phase Reacquisition Control circuit prevents using the phase sample from both sides of the counter wrap-around point when performing the Phase Sample averaging. The Phase Count is first divided in four quadrants, each equal to approximately a quarter of the Phase Count. Comparators are used to determine in which quadrant each phase sample is located. When two successive samples (one in the first quadrant and the other in the last quadrant) are seen, the Reference Phase Alignment Flag (RPHALFLG) is generated.

Upon reception of this signal, the Phase Counter is reset to align the phase count sampling point towards its middle count. This signal is also sent to the Phase Averager circuit. The generation of this signal may be squelched by setting the AUTOREAC bit of the WANS configuration register.

10.20.3 Phase Averager

To provide some noise immunity and improve the resolution of the phase detector algorithm of the WANS, the phase samples are averaged over a programmable number of samples.

Although referred to as an averaging process, it is truly an accumulation process. It retains full resolution, i.e. no division is performed on the accumulated value. The Phase Word includes an integer and a fractional part. The number of averaging samples sets the size of the fractional part.

A programmable counter, the Sample Counter, is incremented at each SAMPLEN signal. This Sample Counter defines the Phase Averaging Period, equal to the Reference Period times the programmed number of phase samples. At the end of this period, the accumulated phase sample value is transferred to the Phase Word register. The Phase Word (PHAWORD) is then accessible by an external processor. A timer flag (TIMFLG) is raised at the end of each averaging period. The flag may be used to generate an interrupt request to an external processor.

Because it indicates that the averaging process includes invalid sample values, the RPHALFLG signal also prevents the Phase Word register from being updated at the end of the current Phase Averaging period. The RPHAFLG signal indicates this event by sending the Reference Phase Alignment condition signal (RPHALGN) to the CBI status register. The RPHALGN signal is reset at the end of the following valid Phase Averaging period.

10.21 ATM UTOPIA and Packet over SONET/SDH POS-PHY System Interfaces

The S/UNI-1x155 system interface can be configured for UTOPIA or POS-PHY modes of operation.

When configured for UTOPIA operation, the S/UNI-1x155 implements a multi-PHY UTOPIA Level 2 interface to allow the transfer of ATM cells between the ATM layer device and the S/UNI-1x155.

When configured for POS-PHY operation, the S/UNI-1x155 implements a multi-PHY POS-PHY Level 2 interface. In this mode, the S/UNI-1x155 supports POS applications.

10.21.1 Receive UTOPIA Level 2 Interface

The UTOPIA Level 2 compliant interface accepts a read clock (RFCLK) and read enable signal (RENB). The interface indicates the start of a cell (RSOC) and the receive cell available status (RCA) when data is read from the receive FIFO (using the rising edges of RFCLK). The RCA status changes from available to unavailable when the FIFO is either empty (when RCALEVEL0 is high) or near empty (when RCALEVEL0 is low). This interface also indicates FIFO overruns via a maskable interrupt and register bits. Read accesses while RCA is a logic zero will output invalid data. The FIFO is reset on FIFO overrun, causing up to 4 cells to be lost.

10.21.2 Receive POS-PHY Level 2 Interface

The POS-PHY Level 2 Interface is an extension to the UTOPIA interface defined for the transfer of ATM cells.

The RSOP signal is used to identify the start of a packet, the RPA signal notifies the system side that data is in the receive FIFO (when a programmable number of bytes in a single packet is received or when an end of packet is available); the RDAT[15:0] bus transfer the data from the FIFO across the system interface; the RPRTY signal determines the parity on the RDAT bus (selectable as odd or even parity); the RFCLK is used to read words from the FIFO interface; and the RENB is used to initiate reads from the receive FIFO. Signal REOP (Receive End of Packet) is used to identify the end of a packet. Signal RMOD (Receive Mod) is provided to indicate whether 1 or 2 bytes are valid on the final word transfer when in 16-bit mode (REOP is asserted). Signal RERR (Receive Error) is provided to indicate that an error in the received packet has occurred (may have several causes, including an abort sequence and an FCS error).

The receive data valid signal, RVAL, plays a special role in this interface. The data signals shall be considered valid only when RVAL is asserted. RVAL is asserted when a data transfer is initiated, conditional to RPA being also asserted. Once the transfer is initiated, RVAL will remain asserted until either the FIFO is empty or an end of packet is encountered. Once deasserted, RVAL will remain low until the current PHY is deselected and another or the same PHY is reselected. RVAL allows the link layer device to align data transfers with packet boundaries, making it easier to manage packet buffers. RVAL should be used at all times when RENB is low to qualify the receive data stream due to RPA falsely indicating data in the FIFO. See the Functional Timing section for more information.

10.21.3 Transmit UTOPIA Level 2 Interface

The UTOPIA Level 2 compliant interface accepts a write clock (TFCLK), a write enable signal (TENB), the start of a cell (TSOC) indication, and the parity bit (TPRTY), when data is written to the transmit FIFO (using the rising edges of TFCLK). The interface provides the transmit cell available status (TCA) which can transition from "available" to "unavailable" when the transmit FIFO is near full (when TCALEVEL0 is low) or when the FIFO is full (when TCALEVEL0 is high) and can accept no more writes. To reduce FIFO latency, the FIFO depth at which TCA indicates "full" can be set to one, two, three or four cells by the FIFODP[1:0] bits of the TXCP Configuration 2 register. If the programmed depth is less than four, more than one cell may be written after TCA is asserted as the TXCP still allows four cells to be stored in its FIFO.

This interface also indicates FIFO overruns via a maskable interrupt and register bit, but write accesses while TCA is low are not processed. The TXCP automatically transmits idle cells until a full cell is available to be transmitted.

10.21.4 Transmit POS-PHY Level 2 Interface

The POS-PHY Level 2 Interface is an extension to the UTOPIA 2 interface defined for the transfer of ATM cells. POS-PHY byte-level transfer mode is supported.

The TSOP signal is used to identify the start of a packet; the TPA signal notify the system side that the transmit FIFO is not full (the POS processor will not start transmitting a packet until a programmable number of bytes for a single packet or the entire packet is in the FIFO; the TDAT[15:0] bus transfer the data to the FIFO from the system interface; the TPRTY signal determines the parity on the TDAT bus (selectable as odd or even parity); the TFCLK is used to write words to the FIFO interface; and finally the TENB is used to initiate writes to the transmit FIFO. The TXCP automatically transmits idle flag characters until sufficient data is available in the transmit FIFO to start transmission.

The TEOP signal (Transmit End of Packet) is used to identify the end of a packet. The TMOD signal (Transmit Mod) is provided to indicate whether 1 or 2 bytes are valid of the final word transfer (TEOP is asserted). TMOD is only valid in 16-bit mode of operation. The TERR signal (Transmit Error) is provided to error a packet that has begun transmission (the packet will be aborted).

10.22 Transmit APS Interface

The Transmit APS interface allows two S/UNI-1x155 devices to exchange SONET/SDH path data streams. The transmit interface generates a SONET/SDH serial data stream with valid section and path overheads This allows performance monitoring and alarm generation to be done in a similar manner to the serial line side interfaces.

The APS path information may be sourced from the receive side of a channel (RSOP/RLOP) or from the transmit side of a channel (TPOP/TXFP/TXCP/TFCLK DLL).

10.22.1 APS Parallel to Serial Converter

The APS Parallel to Serial Converter (APISO) converts each transmit APS byte serial stream to a bit serial stream. The transmit bit serial stream appears on the APSO+/- PECL outputs.

10.23 Transmit APS Overhead Processor

The Transmit APS Overhead Processor (TAOP) provides frame pattern insertion (A1, A2), scrambling and section BIP-8 (B1) insertion on the APS output stream. The processor is similar to a Transmit Section Overhead processor (TSOP) except some features of the TSOP are not supported.

10.23.1 Data Link Insert

The section DCC bytes (D1, D2 and D3) are used to imbed the transport alarm (section and/or line alarms) status of the path data into the APS stream. When the section or line overheads of the path data stream is in alarm condition (LOS, LOF, LAIS, LRDI or LOP), the DCC bytes are set to all ones (0xFF). The DCC bytes are set to all zeros (0x00) when the section and line overheads of the path data stream are not in alarm condition.

10.23.2 BIP-8 Insert

The BIP-8 calculation is based on the scrambled data of the complete APS frame. The section BIP-8 code is based on a bit interleaved parity calculation using even parity. Details are provided in the references. The calculated BIP-8 code is then inserted into the B1 byte of the following frame before scrambling. BIP-8 errors may be continuously inserted under register control for diagnostic purposes.

10.23.3 Framing and Identity Insert

The Framing and Identity Insert Block inserts the framing bytes (A1, A2) into the APS frame. Framing bit errors may be continuously inserted under register control for diagnostic purposes.

10.23.4 Scrambler

The Scrambler Block utilizes a frame synchronous scrambler to process the transmit stream when enabled through an internal register accessed via the microprocessor interface. The generating polynomial is $x^7 + x^6 + 1$. Precise details of the scrambling operation are provided in the references. Note that the framing bytes are not scrambled. All zeros may be continuously inserted (after scrambling) under register control for diagnostic purposes.

10.24 SONET/SDH Path Aligner

The SONET/SDH Path Aligner (STAL) synchronizes the transmit APS path data streams to the CSU transmit clock domain. All APS bit serial interfaces are transmitted using the synthesized 155.52 MHz clock from the CSU and require all APS path data streams to be aligned to this clock domain.

Frequency offsets (due to receive path information) and phase differences (due to normal network operation) between a channel's path stream and the APS stream are accommodated by pointer adjustments on the APS stream. The alignment is accomplished by recalculating the SONET/SDH payload pointer value based on the offset between transport overhead of the path data stream and the outgoing APS data stream.

Since each STAL only processes a STS-1/STM-0 pointer, the APS interface uses one master STAL block to process the concatenated payload pointers and 2 other slave STAL blocks to handle the remaining STS-1/STM-0 data streams.

10.25 Receive APS Interface

The Receive APS interface (RAPS) allows two S/UNI-1x155 devices to exchange SONET/SDH path data streams. The receive interface accepts a SONET/SDH serial data stream with valid section and path overheads ignoring all line overhead information. This allows performance monitoring and alarm generation to be done in a similar manner to the serial line side interfaces.

The APS path information may be terminated by the receive side of a channel (RPOP/RXCP/RXFP) or inserted into the transmit side of a channel (TSOP/TLOP).

10.25.1 APS Data Recovery Unit

The data and clock recovery unit (DCRU) recovers the data from the incoming 155 Mbit/s APS serial stream. The DCRU adapts the 155.52 MHz free running clock from the CSU to recover the incoming APS bit serial. In order for the DCRU to lock to the incoming stream, the APS link must be frequency locked to the CSU 155.52 MHz clock. Low frequency jitter, such as temperature induced wander, may be tracked by the DCRU. Input APS port wander is a result of phase noise or transient between the APS port timings of the Working and Protect devices which should not exceed more than 15UI pp. The APS jitter performance of the S/UNI-1x155 is compliant with Bellcore GR-253-CORE (1995 Issue) SONET and SDH jitter requirements.

10.25.2 APS Serial to Parallel Converter

The APS Serial to Parallel Converter (SIPO) searches for the initial SONET/SDH framing pattern in the receive APS stream, and performs serial to parallel conversion on octet boundaries.

While out of frame, the SIPO block monitors the recovered APS data stream for an occurrence of a A1 byte. The SIPO adjusts its byte alignment of the serial-to-parallel converter when three consecutive A1 bytes followed by three consecutive A2 bytes occur in the data stream. The SIPO informs the RAOP Framer block when this framing pattern has been detected to reinitializes the RAOP to the new frame alignment.

While in frame, the SIPO maintains the byte alignment APS data stream until AROP declares out of frame.

10.26 Receive APS Overhead Processor

The Receive APS Overhead Processor (RAOP) provides frame synchronization, descrambling, section level alarm and performance monitoring. The processor is similar to a Receive Section Overhead processor (RSOP) except some features of the RSOP are not supported.

10.26.1 Framer

The Framer Block determines the in-frame/out-of-frame status of the receive APS stream. While in-frame, the framing bytes (A1, A2) in each frame are compared against the expected pattern. Out-of-frame is declared when four consecutive frames containing one or more framing pattern errors have been received.

While out of frame, the RAPS block monitors the bit-serial APS data stream for an occurrence of the framing pattern (A1, A2). The RAPS informs the RAOP Framer block when three A1 bytes followed by three A2 bytes has been detected to reinitializes the frame byte counter to the new alignment. The Framer block declares frame alignment on the next SONET/SDH frame when either all A1 and A2 bytes are seen error-free or when only the first A1 byte and the first four bits of the last A2 byte are seen error-free depending upon the selected framing algorithm.

Once in frame, the Framer block monitors the framing pattern sequence and declares out of frame (OOF) when one or more bit errors in each framing pattern are detected for four consecutive frames. Again, depending upon the algorithm either all framing bytes are examined for bit errors each frame, or only the first A1 byte and the first four bits of the last A2 byte are examined for bit errors each frame.

10.26.2 Descramble

The Descramble Block utilizes a frame synchronous descrambler to process the receive stream. The generating polynomial is $x^7 + x^6 + 1$ and the sequence length is 127. Details of the descrambling operation are provided in the references. Note that the framing bytes (A1 and A2) are not descrambled. A register bit is provided to disable the descrambling operation.

10.26.3 Data Link Extract

The section DCC bytes (D1, D2 and D3) are used to indicate transport alarm (section and/or line alarms) status of the path data stream. When 3 of 5 bits of the DCC data stream are high, the path data stream is in transport alarm condition (LOS, LOF, LAIS, LRDI or LOP). When 3 of 5 bits of the DCC data stream are low, the path data stream is not in alarm condition.

When the APS path data stream is used by the transmit serial interface (transmit path bridged from a remote S/UNI-1x155 to a transmit channel), a transport alarm will cause path AIS to be inserted in the transmit direction.

When the APS path data stream is terminated by the receive serial interface (receive path from a remove S/UNI-1x155 selected by a receive channel), a transport alarm will affect the AUTOPRDI function in the path transmit direction.

10.26.4 Error Monitor

The Error Monitor Block calculates the received section BIP-8 error detection code (B1) based on the scrambled data of the complete SONET/SDH frame. The section BIP-8 code is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 code is compared with the BIP-8 code extracted from the B1 byte of the following frame. Differences indicate that a section level bit error has occurred. Up to 64000 (8 x 8000) bit errors can be detected per second.

The Error Monitor Block accumulates these section level bit errors in a 16-bit saturating counter that can be read via the microprocessor interface. Circuitry is provided to latch this counter so that its value can be read while simultaneously resetting the internal counter to 0 or 1, if appropriate, so that a new period of accumulation can begin without loss of any events. It is intended that this counter be polled at least once per second so as not to miss bit error events.

10.26.5 Loss of Signal

The Loss of Signal Block monitors the scrambled data of the receive stream for the absence of 1's or 0's. When 20 ± 3 µs of all zeros patterns or all ones patterns are detected, a loss of signal (LOS) is declared. Loss of signal is cleared when two valid framing words are detected and during the intervening time, no loss of signal condition is detected. The APS path stream is forced to all ones (PAIS) when LOS occurs.

10.26.6 Loss of Frame

The Loss of Frame Block monitors the in-frame / out-of-frame status of the Framer Block. A loss of frame (LOF) is declared when an out-of-frame (OOF) condition persists for 3 ms. The LOF is cleared when an in-frame condition persists for a period of 3 ms. To provide for intermittent out-of-frame (or in-frame) conditions, the 3 ms timer is not reset to zero until an in-frame (or out-of-frame) condition persists for 3 ms. The APS path stream is forced to all ones (PAIS) when OOF or LOF occurs.

10.27 Channel Cross Connect

The Channel Cross Connect allows the channel to exchange path information with the APS serial interface. For all configurations, the transmit and receive path processors (RPOP and TPOP) are a matched set and exchange path FEBE and RDI information.

In the transmit direction, the cross connect allows the channels to transmit ATM/POS data or allow the channel to transmit receive APS path data streams (protection channel function).

In the receive direction, the cross connect allows the receive path processor (RPOP) to select between receive channel and APS path data stream (select between working and protection channels).

10.28 JTAG Test Access Port

The JTAG Test Access Port block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST instructions are supported. The S/UNI-1x155 identification code is 0x053840CD hexadecimal.

10.29 Microprocessor Interface

The microprocessor interface block provides normal and test mode registers, and the logic required to connect to the microprocessor interface. The normal mode registers are required for normal operation, and test mode registers are used to enhance the testability of the S/UNI-1x155. In the following section every register is documented and identified using the register number.

11 Normal Mode Register Description

Normal mode registers are used to configure and monitor the operation of the S/UNI-1x155 and are selected when TRS (A[7]) is low.

Test mode registers are used to enhance the testability of the S/UNI-1x155. Refer to section 12 for information about test registers.

11.1 Register Memory Map

The register set is accessed as described in Table 8, which describes every normal mode register for the channel's address space.

Table 8 Register Memory Map

Address	Register Description
000	S/UNI-1x155 Master Reset and Identity
001	S/UNI-1x155 Master Configuration
002	Reserved
003	Reserved
004	Channel Master Configuration #1
005	Channel Master Configuration #2
006	Channel Reset/Interrupt Status #1
007	Channel Master Interrupt Status #2
008	Channel Auto Line RDI Control
009	Channel Auto Path RDI Control
00A	Channel Auto Enhanced Path RDI Control
00B	Channel Receive RDI and Enhanced RDI Control
00C	Channel Receive Line AIS Control
00D	Channel Receive Path AIS Control
00E	Channel Receive Alarm Control #1
00F	Channel Receive Alarm Control #2
010	RSOP Control/Interrupt Enable
011	RSOP Status/Interrupt Status
012	RSOP Section BIP-8 LSB
013	RSOP Section BIP-8 MSB
014	TSOP Control
015	TSOP Diagnostic
016	TSOP Reserved
017	TSOP Reserved
018	RLOP Control/Status
019	RLOP Interrupt Enable/Interrupt Status
01A	RLOP Line BIP-24 LSB

Address	Register Description
01B	RLOP Line BIP-24
01C	RLOP Line BIP-24 MSB
01D	RLOP Line FEBE LSB
01E	RLOP Line FEBE
01F	RLOP Line FEBE MSB
020	TLOP Control
021	TLOP Diagnostic
022	TLOP Transmit K1
023	TLOP Transmit K2
024	TLOP Transmit Synchronization Message (S1)
025	TLOP Transmit J0/Z0
026	Reserved
027	Reserved
028	SSTB Control
029	SSTB Section Trace Identifier Status
02A	SSTB Indirect Address Register
02B	SSTB Indirect Data Register
02C	SSTB Reserved
02D	SSTB Reserved
02E	SSTB Indirect Access Trigger Register
02F	SSTB Reserved
030	RPOP Status/Control (EXTD=0)
030	RPOP Status/Control (EXTD=1)
031	RPOP Interrupt Status (EXTD=0)
031	RPOP Interrupt Status (EXTD=1)
032	RPOP Pointer Interrupt Status
033	RPOP Interrupt Enable (EXTD=0)
033	RPOP Interrupt Enable (EXTD=1)
034	RPOP Pointer Interrupt Enable
035	RPOP Pointer LSB
036	RPOP Pointer MSB
037	RPOP Path Signal Label
038	RPOP Path BIP-8 LSB
039	RPOP Path BIP-8 MSB
03A	RPOP Path FEBE LSB
03B	RPOP Path FEBE MSB
03C	RPOP RDI
03D	RPOP Ring Control
03E	RPOP Reserved
03F	RPOP Reserved

Address	Register Description
040	TPOP Control/Diagnostic
041	TPOP Pointer Control
042	TPOP Reserved
043	TPOP Current Pointer LSB
044	TPOP Current Pointer MSB
045	TPOP Arbitrary Pointer LSB
046	TPOP Arbitrary Pointer MSB
047	TPOP Path Trace
048	TPOP Path Signal Label
049	TPOP Path Status
04A	TPOP Reserved
04B	TPOP Reserved
04C	TPOP Reserved
04D	TPOP Reserved
04E	TPOP Concatenation LSB
04F	TPOP Concatenation MSB
050	SPTB Control
051	SPTB Path Trace Identifier Status
052	SPTB Indirect Address Register
053	SPTB Indirect Data Register
054	SPTB Expected Path Signal Label
055	SPTB Path Signal Label Status
056	SPTB Indirect Access Trigger Register
057	SPTB Reserved
058	DCRU Configuration
059	DCRU Reserved
05A	DCRU Reset
05B	DCRU Reserved
05C	CRSI Configuration
05D	CRSI Status
05E	CRSI Reserved
05F	Unused
060	RXCP Configuration 1
061	RXCP Configuration 2
062	RXCP FIFO/UTOPIA Control and Configuration
063	RXCP Interrupt Enable and Count Status
064	RXCP Status/Interrupt Status
065	RXCP LCD Count Threshold LSB
066	RXCP LCD Count Threshold MSB
067	RXCP Idle Cell Header Pattern

Address	Register Description
068	RXCP Idle Cell Header Mask
069	RXCP Reserved
06A	RXCP HCS Error Count
06B	RXCP Received Cell Count LSB
06C	RXCP Received Cell Count
06D	RXCP Received Cell Count MSB
06E	RXCP Idle Cell Count LSB
06F	RXCP Idle Cell Count
070	RXCP Idle Cell Count MSB
071	RXCP Reserved
072	RXCP Reserved
073	RXCP Reserved
074	RXCP Reserved
075	RXCP Reserved
076	RXCP Reserved
077	RXCP Reserved
078	RXCP Reserved
079	RXCP Reserved
07A	RXCP Reserved
07B	RXCP Reserved
07C	RXCP Reserved
07D	RXCP Reserved
07E	RXCP Reserved
07F	RXCP Reserved
080	TXCP Configuration 1
081	TXCP Configuration 2
082	TXCP Transmit Cell Count Status
083	TXCP Interrupt Enable/Status
084	TXCP Idle Cell Header Control
085	TXCP Idle Cell Payload Control
086	TXCP Transmit Cell Count LSB
087	TXCP Transmit Cell Count
088	TXCP Transmit Cell Count MSB
089	TXCP Reserved
08A	TXCP Reserved
08B	TXCP Reserved
08C	TXCP Reserved
08D	TXCP Reserved
08E	TXCP Reserved
08F	TXCP Reserved

Address	Register Description
090	BIDXReserved
091	BIDX Reserved
092-093	Unused
094	Receive Performance Count LSB
095	Receive Performance Count
096	Receive Performance Count MSB
097	Unused
098	JAT Configuration #1
099	JAT Configuration #2
09A	JAT Reset
09B	JAT Reserved
09C-09F	Unused
0A0	RXFP Configuration
0A1	RXFP Configuration/Interrupt Enable
0A2	RXFP Interrupt Status
0A3	RXFP Minimum Packet Length
0A4	RXFP Maximum Packet Length LSB
0A5	RXFP Maximum Packet Length MSB
0A6	RXFP Receive Initiation Level
0A7	RXFP Receive Packet Available High Mark
0A8	RXFP Receive Byte Counter LSB
0A9	RXFP Receive Byte Counter
0AA	RXFP Receive Byte Counter
0AB	RXFP Receive Byte Counter MSB
0AC	RXFP Receive Frame Counter LSB
0AD	RXFP Receive Frame Counter
0AE	RXFP Receive Frame Counter MSB
0AF	RXFP Aborted Frame Count LSB
0B0	RXFP Aborted Frame Count MSB
0B1	RXFP FCS Error Frame Count LSB
0B2	RXFP FCS Error Frame Count MSB
0B3	RXFP Minimum Length Frame Count LSB
0B4	RXFP Minimum Length Frame Count MSB
0B5	RXFP Maximum Length Frame Count LSB
0B6	RXFP Maximum Length Frame Count MSB
0B7	RXFP Reserved
0B8	RXFP Reserved
0B9	RXFP Reserved
0BA	RXFP Reserved
0BB	RXFP Reserved

Address	Register Description
0BC	RXFP Reserved
0BD	RXFP Reserved
0BE	RXFP Reserved
0BF	RXFP Reserved
0C0	TXFP Interrupt Enable/Status
0C1	TXFP Configuration
0C2	TXFP Control
0C3	TXFP Transmit Packet Available Low Water Mark
0C4	TXFP Transmit Packet Available High Water Mark
0C5	TXFP Transmit Byte Count LSB
0C6	TXFP Transmit Byte Count
0C7	TXFP Transmit Byte Count
0C8	TXFP Transmit Byte Count MSB
0C9	TXFP Transmit Frame Count LSB
0CA	TXFP Transmit Frame Count
0CB	TXFP Transmit Frame Count MSB
0CC	TXFP Transmit User Aborted Frame Count LSB
0CD	TXFP Transmit User Aborted Frame Count MSB
0CE	TXFP Transmit Underrun Aborted Frame Count LSB
0CF	TXFP Transmit Underrun Aborted Frame Count MSB
0D0	WANS Configuration
0D1	WANS Interrupt and Status
0D2	WANS Phase Word LSB
0D3	WANS Phase Word
0D4	WANS Phase Word
0D5	WANS Phase Word MSB
0D6	WANS Reserved
0D7	WANS Reserved
0D8	WANS Reserved
0D9	WANS Reference Period LSB
0DA	WANS Reference Period MSB
0DB	WANS Phase Counter Period LSB
0DC	WANS Phase Counter Period MSB
0DD	WANS Phase Average Period
0DE	WANS Reserved
0DF	WANS Reserved
0E0	RASE Interrupt Enable
0E1	RASE Interrupt Status
0E2	RASE Configuration/Control
0E3	RASE SF BERM Accumulation Period LSB

Address	Register Description
0E4	RASE SF BERM Accumulation Period
0E5	RASE SF BERM Accumulation Period MSB
0E6	RASE SF BERM Saturation Threshold LSB
0E7	RASE SF BERM Saturation Threshold MSB
0E8	RASE SF BERM Declaring Threshold LSB
0E9	RASE SF BERM Declaring Threshold MSB
0EA	RASE SF BERM Clearing Threshold LSB
0EB	RASE SF BERM Clearing Threshold MSB
0EC	RASE SD BERM Accumulation Period LSB
0ED	RASE SD BERM Accumulation Period
0EE	RASE SD BERM Accumulation Period MSB
0EF	RASE SD BERM Saturation Threshold LSB
0F0	RASE SD BERM Saturation Threshold MSB
0F1	RASE SD BERM Declaring Threshold LSB
0F2	RASE SD BERM Declaring Threshold MSB
0F3	RASE SD BERM Clearing Threshold LSB
0F4	RASE SD BERM Clearing Threshold MSB
0F5	RASE Receive K1
0F6	RASE Receive K2
0F7	RASE Receive Z1/S1
0F8	BIDX Reserved
0F9	BIDX Reserved
0FA	BIMX Reserved
0FB	BIMX Reserved
0FC	Channel Concatenation Status and Enable
0FD	Channel Concatenation Interrupt Status
0FE	Channel Serial Interface Configuration
0FF	Channel Clock Monitors
100	S/UNI-1x155 Master Interrupt Status
101	S/UNI-1x155 DCC Interface Configuration
102	CSPI Clock Synthesis Configuration
103	Unused
104	Unused
105	Unused
106-107	Unused
108	TFCLK DLL Configuration
109	TFCLK DLL Reserved
10A	TFCLK DLL Reset
10B	TFCLK DLL Control Status
10C	RFCLK DLL Configuration

Address	Register Description
10D	RFCLK DLL Reserved
10E	RFCLK DLL Reset
10F	RFCLK DLL Control Status
110	APS Configuration and Status
111	APS Reserved
112	APS Interrupt Status
113	APS Reset Control
114	TAOP APS Link Control
115	TAOP APS Link Diagnostic
116	TAOP APS Link Reserved
117	TAOP APS Link Reserved
118	RAOP APS Link Control/Interrupt Enable
119	RAOP APS Link Status/Interrupt Status
11A	RAOP APS Link Section BIP-8 LSB
11B	RAOP APS Link Section BIP-8 MSB
11C	RAPS APS Link Configuration
11D	RAPS APS Link Status
11E	RAPS APS Link Reserved
11F	RAPS APS Link Reserved
120	DRU Configuration
121	DRU Reserved
122	DRU Reset
123	DRU Reserved
124-12F	Unused
130	Level 2 Receive Address
131	Level 2 Transmit Address
132	Channel Receive Connect Select
133	Channel Transmit Connect Select
134	Channel Connect Control
135-137	Unused
138	STAL Channel Configuration
139	STAL Channel Control and Interrupt Status
13A	STAL Channel Alarm and Diagnostic Control
13B	STAL Channel Reserved
13C	STAL Slave #1 Configuration
13D	STAL Slave #1 Control and Interrupt Status
13E	STAL Slave #1 Alarm and Diagnostic Control
13F	STAL Slave #1 Reserved
140	STAL Slave #2 Configuration
141	STAL Slave #2 Control and Interrupt Status

Address	Register Description
142	STAL Slave #2 Alarm and Diagnostic Control
143	STAL Slave #2 Reserved
144-1FF	Unused
200-3FF	Reserved for Test

Notes on Register Memory Map:

1. For all register accesses, CSB must be low.
2. Addresses that are not shown must be treated as Reserved.
3. A[9] is the test resister select (TRS) and should be set low for normal mode register access.
4. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence, unused register bits should be masked off by software when read.
5. All configuration bits that can be written into can also be read back. This allows the processor controlling the S/UNI-1x155 to determine the programming state of the block.
6. Writable normal mode register bits are cleared to logic zero upon reset unless otherwise noted.
7. Writing into read-only normal mode register bit locations does not affect S/UNI-1x155 operation unless otherwise noted. Performance monitoring counter registers are a common exception.
8. Certain register bits are reserved. These bits are associated with megacell functions that are unused in this application. To ensure that the S/UNI-1x155 operates as intended, reserved register bits must be written with their default value as indicated by the register bit description.
9. Writing any data to the Master Reset and Identity register (0x000) simultaneously loads all the performance monitoring registers in RSOP, RLOP, RPOP, SPTB, SSTB, RXCP, TXCP, RXFP, TXFP and RAOP blocks in the device.

   Writing to the channel Interrupt Status register (0x007) will simultaneously load all the performance monitor registers in RSLOP, RLOP, RPOP, SPTB, SSTB, RXCP, TXCP, RXFP and TXFP blocks .

   Writing any data to the performance register in question may individually trigger the performance registers in each block. In some cases, all performance registers in the block are loaded. In other cases, only the specific register being written will load. See the register descriptions for the performance register in question for more information.

11.2 Registers

Register 0x000: S/UNI-1x155 Master Reset and Identity

Bit	Type	Function	Default
Bit 7	R/W	RESET	0
Bit 6	R	TYPE[3]	0
Bit 5	R	TYPE[2]	0
Bit 4	R	TYPE[1]	1
Bit 3	R	TYPE[0]	0
Bit 2	R	ID[2]	0
Bit 1	R	ID[1]	0
Bit 0	R	ID[0]	0

This register allows the revision number of the S/UNI-1x155 to be read by software permitting graceful migration to newer, feature-enhanced versions of the S/UNI-1x155.

In addition, writing to this register simultaneously loads all the performance monitor registers (equivalent to writing to 0x007.). The TIP register in 0x001 is set high while the performance registers are loaded and clears when the transfer is done.

ID[2:0]:

The ID bits can be read to provide a binary S/UNI-1x155 revision number.

TYPE[3:0]:

The TYPE bits can be read to distinguish the S/UNI-1x155 from the other members of the S/UNI family of devices.RESET:

The RESET bit allows the S/UNI-1x155 to be reset under software control. If the RESET bit is a logic one, the entire S/UNI-1x155 is held in reset. This bit is not self-clearing. Therefore, a logic zero must be written to bring the S/UNI-1x155 out of reset. Holding the S/UNI-1x155 in a reset state places it into a low power, stand-by mode. A hardware reset clears the RESET bit, thus negating the software reset. Otherwise, the effect of a software reset is equivalent to that of a hardware reset.

Register 0x001: S/UNI-1x155 Master Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	ATM8	0
Bit 0	R	TIP	X

TIP:

The TIP bit is set to a logic one when the performance monitor registers are being loaded. Writing to the S/UNI-1x155 Master Reset and Identity register (0x000) initiates an accumulation interval transfer and loads all the performance monitor registers in the RSOP, RLOP, RPOP, SSTB, SPTB, RXCP, TXCP, RXFP, TXFP and RAOP blocks.

TIP remains high while the transfer is in progress, and is set to a logic zero when the transfer is complete. TIP can be polled by a microprocessor to determine when the accumulation interval transfer is complete.

ATM8:

The 8-bit interface enable (ATM8) configures the system interface to operate using the 8-bit UTOPIA Level 2 protocol. When ATM8 is set high the device operates in ATM mode using the 8-bit UTOPIA Level 2 interface.

Register 0x004: Channel Master Configuration #1

Bit	Type	Function	Default
Bit 7	R/W	TPTBEN	0
Bit 6	R/W	TSTBEN	0
Bit 5	R/W	SDH_J0/Z0	0
Bit 4	R/W	TFPEN	0
Bit 3	R/W	DLE	0
Bit 2	R/W	PDLE	0
Bit 1	R/W	Reserved	0
Bit 0	R	CHTIP	X

CHTIP:

The CHTIP bit is set to a logic one when the channel's performance monitor registers are being loaded. Writing to the channel's Interrupt Status #2 register (0x007) initiates an accumulation interval transfer and loads all the performance monitor registers in the channel's RSOP, RLOP, RPOP, SSTB, SPTB, RXCP, TXCP, RXFP and TXFP blocks.

Writing to the S/UNI-1x155 Master Reset and Identity register (0x000) will cause the channel to load the performance monitor registers. This operation is equivalent to writing to the Interrupt Status #2 register (0x007).

CHTIP remains high while the transfer is in progress, and is set to a logic zero when the transfer is complete. CHTIP can be polled by a microprocessor to determine when the accumulation interval transfer is complete.

PDLE:

The Parallel Diagnostic Loopback, PDLE bit enables the channel's diagnostic loopback where the channel's Transmit Section Overhead Processor (TSOP) is directly connected to its Receive Section Overhead Processor (RSOP). When PDLE is logic one, loopback is enabled. Under this operating condition, the channel continues to operate normally in the transmit direction. When PDLE is logic zero, the channel operates normally in both directions.

DLE:

The Diagnostic Loopback, DLE bit enables the channel's diagnostic loopback where the channel's Transmit ATM and POS Processors (TXCP and TXFP respectively) are directly connected to the Receive ATM and POS Processor (RXCP and RXFP respectively). When DLE is logic one, loopback is enabled. Under this operating condition, the channel does not operate normally in the transmit direction or receive direction. When DLE is logic zero, the channel operates normally.

The receive APS enable RXEN must be low while DLE is high in order for the loopback to operate correctly.

TFPEN:

The Transmit Frame Pulse Enable (TFPEN) enables the TFPI input. When TFPEN is set low, the channel ignores the TFPI input. When TFPEN is set high, the TFPI input is used by the channel for frame alignment.

SDH_J0/Z0

The SDH_J0/Z0 bit selects whether to insert SONET or SDH format J0/Z0 section overhead bytes into the transmit stream. When SDH_J0/Z0 is set high, SDH format J0/Z0 bytes are selected for insertion. For this case, all the J0/Z0 bytes are forced to the value programmed in the channel's Transmit J0/Z0 register. When SDH_J0/Z0 is set low, SONET format J0/Z0 bytes are selected for insertion. For this case, the J0/Z0 bytes of an STS-N signal are numbered incrementally from 1 to N.

TSTBEN can be used to overwrite the first J0/Z0 byte of an STS-N signal.

TSTBEN:

The TSTBEN bit controls whether the section trace message stored in the SSTB block is inserted into the transmit stream (i.e., the first J0/Z0 byte). When TSTBEN is set high the message stored in the SSTB is inserted into the transmit stream. When TSTBEN is set low the section trace message is supplied by the TSOP block.

TPTBEN:

The TPTBEN bit controls whether the path trace message stored in the SPTB block is inserted into the transmit stream (i.e., the J1 byte). When TPTBEN is set high, the message stored in the SPTB is inserted into the transmit stream. When TPTBEN is set low, the path trace message is supplied by the TPOP block.

Reserved:

The reserved bit must be programmed to logic zero for proper operation.

Register 0x005: Channel Master Configuration #2

Bit	Type	Function	Default
Bit 7	R/W	SLLE	0
Bit 6	R/W	SDLE	0
Bit 5	R/W	LOOPT	0
Bit 4	R/W	DPLE	0
Bit 3	R/W	AUTOLRDI	1
Bit 2	R/W	AUTOPRDI	1
Bit 1	R/W	AUTOLFEBE	1
Bit 0	R/W	AUTOPFEBE	1

For more details refer to the Operation Section of this document.

AUTOPFEBE

The AUTOPFEBE bit determines if the remote path block errors are sent upon detection of an incoming path BIP error event. When AUTOPFEBE is set to logic one, one path FEBE is inserted for each path BIP error event, respectively. When AUTOPFEBE is set to logic zero, incoming path BIP error events do not generate FEBE events.

AUTOLFEBE

The AUTOLFEBE bit determines if remote line block errors are sent upon detection of an incoming line BIP error event. When AUTOLFEBE is set to logic one, one line FEBE is inserted for each line BIP error event, respectively. When AUTOLFEBE is set to logic zero, incoming line BIP error events do not generate FEBE events.

AUTOPRDI

The AUTOPRDI bit determines whether STS path remote defect indication (RDI) is sent immediately upon detection of an incoming alarm. When AUTOPRDI is set to logic one, STS path RDI is inserted immediately upon declaration of several alarms. Each alarm can individually be enabled and disabled using the channel's Path RDI Control Registers.

AUTOLRDI

The AUTOLRDI bit determines if line remote defect indication (RDI) is sent immediately upon detection of an incoming alarm. When AUTOLRDI is set to logic one, line RDI is inserted immediately upon declaration of several alarms. Each alarm can individually be enabled and disabled using the channel's Line RDI Control Registers.

DPLE:

The Diagnostic Path Loopback, DPLE bit enables the channel's diagnostic loopback where channel's Transmit Path Overhead Processor (TPOP) is directly connected to its Receive Path Overhead Processor (RPOP). When DPLE is logic one, loopback is enabled. Under this operating condition, the channel continues to operate normally in the transmit direction. When DPLE is logic zero, the channel operates normally.

LOOPT:

The LOOPT bit selects the source of timing for the transmit section of the channel. When LOOPT is a logic zero, the transmitter timing is derived from input REFCLK (CSU). When LOOPT is a logic one, the transmitter timing is derived from the recovered clock (Clock Recovery Unit). LOOPT should not be set if the WANS is being used. The SDLE or LOOPT bits should not be set high simultaneously.

SDLE:

The SDLE bit enables the serial diagnostic loopback. When SDLE is a logic one, the channel's transmit serial stream on the TXD+/- differential outputs is internally connected to the received serial RXD+/- differential inputs. Under this operating condition, the channel continues to operate normally in the transmit direction. The SDLE, SLLE or LOOPT bits should not be set high simultaneously.

SLLE:

The SLLE bit enables the channel's line loopback mode. When SLLE is a logic one, the channel's recovered data from the receive serial RXD+/- differential inputs is mapped to the TXD+/- differential outputs. Under this operating condition, the channel continues to operate normally in the receive direction. The LOOPT bits must also be set high when SLLE is set high for proper operation.

Register 0x006: Channel Reset/Master Interrupt Status #1

Bit	Type	Function	Default
Bit 7	R/W	CHRST	0
Bit 6	R	CONCATI	X
Bit 5	R	RASEI	X
Bit 4	R	TXCPI	X
Bit 3	R	RXCPI	X
Bit 2	R	RPOPI	X
Bit 1	R	RLOPI	X
Bit 0	R	RSOPI	X

When the interrupt output INTB goes low, this register allows the source of the active interrupt to be identified down to the block level for the channel. Further register accesses are required for the block in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

RSOPI:

The RSOPI bit is high when an interrupt request is active from the RSOP block. The RSOP interrupt sources are enabled in the RSOP Control/Interrupt Enable Register.

RLOPI:

The RLOPI bit is high when an interrupt request is active from the RLOP block. The RLOP interrupt sources are enabled in the RLOP Interrupt Enable/Status Register.

RPOPI:

The RPOPI bit is high when an interrupt request is active from the RPOP block. The RPOP interrupt sources are enabled in the RPOP Interrupt Enable Register.

RXCPI:

The RXCPI bit is high when an interrupt request is active from the RXCP block. The RXCP interrupt sources are enabled in the RXCP Interrupt Enable/Status Register.

TXCPI:

The TXCPI bit is high when an interrupt request is active from the TXCP block. The TXCP interrupt sources are enabled in the TXCP Interrupt Control/Status Register.

RASEI:

The RASEI bit is high when an interrupt request is active from the RASE block. The RASE interrupt sources are enabled in the RASE Interrupt Enable Register.

CONCATI:

The CONCATI bit is high when an interrupt request is active from the Concatenation Interrupt Status Register. The CONCAT interrupt sources are enabled in the Concatenation Status and Enable Register.

CHRST:

The CHRST bit allows the channel to be reset under software control. If the CHRST bit is a logic one, the entire channel is held in reset. This bit is not self-clearing. Therefore, a logic zero must be written to bring the channel out of reset. Holding the channel in a reset state places it into a low power, stand-by mode. A hardware reset or top level reset using RESET clears the CHRST bit, thus negating the software reset. Otherwise, the effect of the channel software reset is equivalent to that of a hardware reset.

Register 0x007: Channel Master Interrupt Status #2

Bit	Type	Function	Default
Bit 7	R	JATI	X
Bit 6	R	DCRUI	X
Bit 5	R	CRSII	X
Bit 4	R	TXFPI	X
Bit 3	R	RXFPI	X
Bit 2	R	WANSI	X
Bit 1	R	SSTBI	X
Bit 0	R	SPTBI	X

When the interrupt output INTB goes low, this register allows the source of the active interrupt to be identified down to the block level for the channel. Further register accesses are required for the block in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

In addition, writing to this register simultaneously loads all the performance monitor registers in the channel. The CHTIP bit is set high while the performance registers are loaded and clears when the transfer is done.

SPTBI:

The SPTBI bit is a logic one when an interrupt request is active from the SPTB block. The SPTB interrupt sources are enabled in the SPTB Control Register and the SPTB Path Signal Label Status Register.

SSTBI:

The SSTBI bit is a logic one when an interrupt request is active from the SSTB block. The SSTB interrupt sources are enabled in the SSTB Control Register and the SSTB Synchronization Message Status Register.

WANSI:

The WANSI bit is a logic one when an interrupt request is active from the WANS block. The WANS interrupt sources are enabled in the WANS Interrupt Enable/Status Register.

RXFPI:

The RXFPI bit is high when an interrupt request is active from the RXFP block. The RXFP interrupt sources are enabled in the RXFP Interrupt Enable/Status Register.

TXFPI:

The TXFPI bit is high when an interrupt request is active from the TXFP block. The TXFP interrupt sources are enabled in the TXFP Interrupt Control/Status Register.

CRSII:

The CRSII bit is high when an interrupt request is active from the Clock Recovery and SIPO block (CRSI). The CRSI interrupt sources are enabled in the Clock Recovery Interrupt Control/Status Register.

DCRUI:

The DCRUI bit is high when an interrupt request is active from the DCRU block. The DCRUI interrupt sources are enabled in the DCRU Configuration Register.

JATI:

The JATI bit is high when an interrupt request is active from the JAT block. The JATI interrupt sources are enabled in the JAT Configuration #1 Register.

Register 0x008: Channel Auto Line RDI Control

Bit	Type	Function	Default
Bit 7	R/W	SDLRDI	0
Bit 6	R/W	SFLRDI	0
Bit 5	R/W	LOFLRDI	1
Bit 4	R/W	LOSLRDI	1
Bit 3	R/W	RTIMLRDI	0
Bit 2	R/W	RTIULRDI	0
Bit 1	R/W	LAISLRDI	1
Bit 0		Unused	X

This register controls the auto assertion of the line RDI in TLOP for the entire SONET/SDH stream for a channel. For more details refer to the Operation Section of this document.

LAISLRDI:

The Line Alarm Indication Signal LRDI (LAISLRDI) controls the insertion of a Line RDI in the transmit data stream upon detection of this alarm condition. When LAISLRDI is set high, the transmit line RDI will be inserted. When LAISLRDI is set low, no action is taken. This register bit is used only if the AUTOLRDI register bit is also set high.

RTIULRDI:

The Section Trace Identifier Unstable LRDI (RTIULRDI) controls the insertion of a Line RDI in the transmit data stream upon detection of this alarm condition. When RTIULRDI is set high, the transmit line RDI will be inserted. When RTIULRDI is set low, no action is taken. This register bit is used only if the AUTOLRDI register bit is also set high.

RTIMLRDI:

The Section Trace Identifier Mismatch LRDI (RTIMLRDI) controls the insertion of a Line RDI in the transmit data stream upon detection of this alarm condition. When RTIMLRDI is set high, the transmit line RDI will be inserted. When RTIMLRDI is set low, no action is taken. This register bit is used only if the AUTOLRDI register bit is also set high.

LOSLRDI:

The Loss of Signal LRDI (LOSLRDI) controls the insertion of a Line RDI in the transmit data stream upon detection of this alarm condition. When LOSLRDI is set high, the transmit line RDI will be inserted. When LOSLRDI is set low, no action is taken. This register bit is used only if the AUTOLRDI register bit is also set high.

LOFLRDI:

The Loss of Frame LRDI (LOFLRDI) controls the insertion of a Line RDI in the transmit data stream upon detection of this alarm condition. When LOFLRDI is set high, the transmit line RDI will be inserted. When LOFLRDI is set low, no action is taken. This register bit is used only if the AUTOLRDI register bit is also set high.

SFLRDI:

The Signal Fail BER LRDI (SFLRDI) controls the insertion of a Line RDI in the transmit data stream upon detection of this alarm condition. When SFLRDI is set high, the transmit line RDI will be inserted. When SFLRDI is set low, no action is taken. This register bit is used only if the AUTOLRDI register bit is also set high.

SDLRDI:

The Signal Degrade BER LRDI (SDLRDI) controls the insertion of a Line RDI in the transmit data stream upon detection of this alarm condition. When SDLRDI is set high, the transmit line RDI will be inserted. When SDLRDI is set low, no action is taken. This register bit is used only if the AUTOLRDI register bit is also set high.

Register 0x009: Channel Auto Path RDI Control

Bit	Type	Function	Default
Bit 7	R/W	LCDPRDI	0
Bit 6	R/W	ALRMPRDI	0
Bit 5	R/W	PAISPRDI	1
Bit 4	R/W	PSLMPRDI	1
Bit 3	R/W	LOPPRDI	1
Bit 2	R/W	LOPCONPRDI	1
Bit 1	R/W	PTIUPRDI	1
Bit 0	R/W	PTIMPRDI	1

This register controls the auto assertion of path RDI (G1 bit 5) in the TPOP for the entire SONET/SDH stream for a channel. Also see the Auto Enhanced Path RDI register. For more details refer to the Operation Section of this document.

PTIMPRDI:

The Path Trace Identifier Mismatch PRDI (PTIMPRDI) controls the insertion of a Path RDI in the transmit data stream upon detection of this alarm condition. When PTIMPRDI is set high, the transmit line RDI will be inserted. When PTIMPRDI is set low, no action is taken. This register bit is used only if the AUTOPRDI register bit is also set high.

PTIUPRDI:

The Path Trace Identifier Unstable PRDI (PTIUPRDI) controls the insertion of a Path RDI in the transmit data stream upon detection of this alarm condition. When PTIUPRDI is set high, the transmit line RDI will be inserted. When PTIUPRDI is set low, no action is taken. This register bit is used only if the AUTOPRDI register bit is also set high.

LOPCONPRDI:

The Loss of Pointer Concatenation Indication PRDI (LOPCONPRDI) controls the insertion of a Path RDI in the transmit data stream upon detection of this alarm condition. When LOPCONPRDI is set high, the transmit line RDI will be inserted. When LOPCONPRDI is set low, no action is taken. This register bit is used only if the AUTOPRDI register bit is also set high.

LOPPRDI:

The Loss of Pointer Indication PRDI (LOPPRDI) controls the insertion of a Path RDI in the transmit data stream upon detection of this alarm condition. When LOPPRDI is set high, the transmit path RDI will be inserted. When LOPPRDI is set low, no action is taken. This register bit is used only if the AUTOPRDI register bit is also set high.

PSLMPRDI:

The Path Signal Label Mismatch PRDI (PSLMPRDI) controls the insertion of a Path RDI in the transmit data stream upon detection of this alarm condition. When PSLMPRDI is set high, the transmit path RDI will be inserted. When PSLMPRDI is set low, no action is taken. This register bit is used only if the AUTOPRDI register bit is also set high.

PAISPRDI:

The Path Alarm Indication Signal PRDI (PAISPRDI) controls the insertion of a Path RDI in the transmit data stream upon detection of this alarm condition. When PAISPRDI is set high, the transmit path RDI will be inserted. When PAISPRDI is set low, no action is taken. This register bitsdf is used only if the AUTOPRDI register bit is also set high.

ALRMPRDI:

The Line Alarm Indication Signal PRDI (ALRMPRDI) controls the insertion of a Path RDI in the transmit data stream upon detection of one of the following alarm conditions: Loss of Signal (LOS), Loss of Frame (LOF) and Line Alarm Indication Signal (LAIS). When ALRMPRDI is set high, the transmit path RDI will be inserted When ALRMPRDI is set low, no action is taken. This register bit is used only if the AUTOPRDI register bit is also set high.

LCDPRDI:

The Loss of ATM Cell Delineation Signal PRDI (LCDPRDI) controls the insertion of a Path RDI in the transmit data stream upon detection of this alarm. When LCDPRDI is set high, the transmit path RDI will be inserted. When LCDPRDI is set low, no action is taken. This register bit is used only if the AUTOPRDI register bit is also set high.

Register 0x00A: Channel Auto Enhanced Path RDI Control

Bit	Type	Function	Default
Bit 7	R/W	LCDEPRDI	0
Bit 6	R/W	NOALMEPRDI	0
Bit 5	R/W	NOPAISEPRDI	0
Bit 4	R/W	PSLMEPRDI	1
Bit 3	R/W	NOLOPEPRDI	0
Bit 2	R/W	NOLOPCONEPRDI	0
Bit 1	R/W	TIUEPRDI	0
Bit 0	R/W	TIMEPRDI	1

This register, along with the Channel Auto Path RDI Control register, controls the auto assertion of enhanced path RDI (G1 bit 5, 6 and 7) in the TPOP for the entire SONET/SDH stream. For more details refer to the Operation Section of this document.

TIMEPRDI:

When set high, the TIMEPRDI bit enables enhanced path RDI assertion when path trace message mismatch (TIM) events are detected in the receive stream. When TIMEPRDI is set high and TIM occurs, bit 6 of the G1 byte is set high while bit 7 of the G1 byte is set low.

When TIMEPRDI is set low, trace identifier mismatch events have no effect on path RDI. In addition, this bit has no effect when EPRDI_EN is set low.

TIUEPRDI:

When set high, the TIUEPRDI bit enables enhanced path RDI assertion when path trace message unstable events are detected in the receive stream. When TIUEPRDI is set high and path trace message unstable occurs, bit 6 of the G1 byte is set high while bit 7 of the G1 byte is set low.

When TIUEPRDI is set low, trace identifier unstable events have no effect on path RDI. In addition, this bit has no effect when EPRDI_EN is set low.

NOLOPCONEPRDI:

When set high, the NOLOPCONEPRDI bit disables enhanced path RDI assertion when loss of pointer concatenation (LOPCON) events are detected in the receive stream. When NOLOPCONEPRDI is set high and LOPCON occurs, bit 6 of the G1 byte is set low while bit 7 of the G1 byte is set high. NOLOPCONEPRDI has precedence over PSLMEPRDI, TIUEPRDI, TIMEPRDI and UNEQEPRDI.

When NOLOPCONEPRDI is set low, reporting of enhanced RDI is according to PSLMEPRDI, TIUEPRDI, TIMEPRDI and UNEQEPRDI and the associated alarm states.

NOLOPEPRDI:

When set high, the NOLOPEPRDI bit disables enhanced path RDI assertion when loss of pointer (LOP) events are detected in the receive stream. When NOLOPEPRDI is set high and LOP occurs, bit 6 of the G1 byte is set low while bit 7 of the G1 byte is set high. NOLOPEPRDI has precedence over PSLMEPRDI, TIUEPRDI, TIMEPRDI and UNEQEPRDI.

When NOLOPEPRDI is set low, reporting of enhanced RDI is according to PSLMEPRDI, TIUEPRDI, TIMEPRDI and UNEQEPRDI and the associated alarm states.

PSLMEPRDI:

When set high, the PSLMEPRDI bit enables enhanced path RDI assertion when path signal label mismatch (PSLM) events are detected in the receive stream. When PSLMEPRDI is set high and PSLM occurs, bit 6 of the G1 byte is set high while bit 7 of the G1 byte is set low.

When PSLMEPRDI is set low, path signal label mismatch events have no effect on path RDI. In addition, this bit has no effect when EPRDI_EN is set low.

NOPAISEPRDI:

When set high, the NOPAISEPRDI bit disables enhanced path RDI assertion when the path alarm indication signal state (PAIS) is detected in the receive stream. When NOPAISEPRDI is set high and PAIS occurs, bit 6 of the G1 byte is set low while bit 7 of the G1 byte is set high. NOPAISEPRDI has precedence over PSLMEPRDI, TIUEPRDI, TIMEPRDI and UNEQEPRDI.

When NOPAISEPRDI is set low, reporting of enhanced RDI is according to PSLMEPRDI, TIUEPRDI, TIMEPRDI and UNEQEPRDI and the associated alarm states.

NOALMEPRDI:

When set high, the NOALMEPRDI bit disables enhanced path RDI assertion when loss of signal (LOS), loss of frame (LOF) or line alarm indication signal (LAIS) events are detected in the receive stream. When NOALMEPRDI is set high and one of the listed events occur, bit 6 of the G1 byte is set low while bit 7 of the G1 byte is set high. NOALMEPRDI has precedence over PSLMEPRDI, TIUEPRDI, TIMEPRDI and UNEQEPRDI.

When NOALMEPRDI is set low, reporting of enhanced RDI is according to PSLMEPRDI, TIUEPRDI, TIMEPRDI and UNEQEPRDI and the associated alarm states.

LCDEPRDI:

When set high, the LCDEPRDI bit enables enhanced path RDI assertion when loss of ATM cell delineation (LCD) events are detected in the receive stream. If enabled, when the event occurs, bit 6 of the G1 byte is set high while bit 7 of the G1 byte is set low.

When LCDEPRDI is set low, loss of ATM cell delineation has no effect on path RDI. In addition, this bit has no effect when EPRDI_EN is set low.

Register 0x00B: Channel Receive RDI and Enhanced RDI Control

Bit	Type	Function	Default
Bit 7	R/W	PAISCONPRDI	0
Bit 6	R/W	NOPAISCONEPRDI	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	EPRDI_EN	0
Bit 1	R/W	UNEQPRDI	1
Bit 0	R/W	UNEQEPRDI	1

This register along with the Enhanced Path RDI Control register controls the auto assertion of path RDI (G1 bit 5, 6 and 7) in the TPOP for the entire SONET/SDH stream. For more details refer to the Operation Section of this document.

UNEQEPRDI:

When set high, the UNEQEPRDI bit enables enhanced path RDI assertion when the path signal label in the receive stream indicates unequipped status. When UNEQEPRDI is set high and the path signal label indicates unequipped, bit 6 of the G1 byte is set high while bit 7 of the G1 byte is set low.

When UNEQEPRDI is set low, path signal label unequipped status has no effect on enhanced path RDI.

UNEQPRDI:

When set high, the UNEQPRDI bit enables path RDI assertion when the path signal label in the receive stream indicates unequipped status. When UNEQPRDI is set low, the path signal label unequipped status has no effect on path RDI.

EPRDI_EN:

The EPRDI_EN bit enables the automatic insertion of enhanced RDI in the local transmitter. When EPRDI_EN is a logic one, auto insertion is enabled using the event enable bits in this register. When EPRDI_EN is a logic zero, enhanced path RDI is not automatically inserted in the transmit stream.

The EPRDIEN and EPRDISRC in register 0x040 must also be set to enable enhanced RDI.

NOPAISCONEPRDI:

When set high, the NOPAISCONEPRDI bit disables enhanced path RDI assertion when path AIS concatenation (PAISCON) events are detected in the receive stream. When NOPAISCONEPRDI is set high and PAISCON occurs, bit 6 of the G1 byte is set low while bit 7 of the G1 byte is set high. NOPAISCONEPRDI has precedence over PSLMEPRDI, TIUEPRDI, TIMEPRDI and UNEQEPRDI.

When NOPAISCONEPRDI is set low, reporting of enhanced RDI is according to PSLMEPRDI, TIUEPRDI, TIMEPRDI and UNEQEPRDI and the associated alarm states.

PAISCONPRDI:

When set high, the PAISCONPRDI bit enables path RDI assertion when path AIS concatenation (PAISCON) events are detected in the receive stream. When PAISCONPRDI is set low, path AIS concatenation events have no effect on path RDI.

Register 0x00C: Channel Received Line AIS Control

Bit	Type	Function	Default
Bit 7	R/W	SDINS	0
Bit 6	R/W	SFINS	0
Bit 5	R/W	LOFINS	1
Bit 4	R/W	LOSINS	1
Bit 3	R/W	RTIMINS	0
Bit 2	R/W	RTIUINS	0
Bit 1		Unused	X
Bit 0	R/W	DCCAIS	0

This register controls the auto assertion of the receive line AIS for the entire SONET/SDH stream.

DCCAIS:

The DCCAIS bit enables the insertion of all ones in the section DCC (and the line DCC when loss of frame (LOF) or LOS is declared. When DCCAIS is a logic one, all ones is inserted in RDCC/RACC outputs when LOF or LOS is declared.

RTIUINS:

The RTIUINS bit enables the insertion of line AIS in the receive direction upon the declaration of section trace unstable. If RTIUINS is a logic one, line AIS is inserted into the SONET/SDH frame when the current received section trace identifier message has not matched the previous message for eight consecutive messages. Line AIS is terminated when the current message becomes the accepted message.

RTIMINS:

The RTIMINS bit enables the insertion of line AIS in the receive direction upon the declaration of section trace mismatch. If RTIMINS is a logic one, line AIS is inserted into the SONET/SDH frame when the accepted identifier message differs from the expected message. Line AIS is terminated when the accepted message matches the expected message.

LOSINS:

The LOSINS bit enables the insertion of line AIS in the receive direction upon the declaration of loss of signal (LOS). If LOSINS is a logic one, line AIS is inserted into the SONET/SDH frame when LOS is declared. Line AIS is terminated when LOS is removed.

LOFINS:

The LOFINS bit enables the insertion of Line AIS in the receive direction upon the declaration of loss of frame (LOF). If LOFINS is a logic one, line AIS is inserted into the SONET/SDH frame when LOF is declared. Line AIS is terminated when LOF is removed.

SFINS:

The SFINS bit enables the insertion of line AIS in the receive direction upon the declaration of signal fail (SF). If SFINS is a logic one, path AIS is inserted into the SONET/SDH frame when SF is declared. Path AIS is terminated when SF is removed.

SDINS:

The SDINS bit enables the insertion of line AIS in the receive direction upon the declaration of signal degrade (SD). If SDINS is a logic one, path AIS is inserted into the SONET/SDH frame when SD is declared. Path AIS is terminated when SD is removed.

Register 0x00D: Channel Receive Path AIS Control

Bit	Type	Function	Default
Bit 7	R/W	PAISCONPAIS	1
Bit 6	R/W	LOPCONPAIS	1
Bit 5	R/W	PSLUPAIS	1
Bit 4	R/W	PSLMPAIS	1
Bit 3	R/W	LOPPAIS	1
Bit 2	R/W	Reserved	1
Bit 1	R/W	TIUPAIS	1
Bit 0	R/W	TIMPAIS	1

This register controls the auto assertion of path AIS, which will force a loss of cell delineation by the receive cell processor.

TIMPAIS:

When set high, the TIMPAIS bit enables path AIS insertion when path trace message mismatch (TIM) events are detected in the receive stream. When TIMPAIS is set low, trace identifier mismatch events will not assert path AIS.

TIUPAIS:

When set high, the TIUPAIS bit enables path AIS insertion when path trace message unstable events are detected in the receive stream. When TIUPAIS is set low, trace identifier unstable events will not assert path AIS.

LOPPAIS:

When set high, the LOPPAIS bit enables path AIS insertion when loss of pointer (LOP) events are detected in the receive stream. When LOPPAIS is set low, loss of pointer events will not assert path AIS.

PSLMPAIS:

When set high, the PSLMPAIS bit enables path AIS insertion when path signal label mismatch (PSLM) events are detected in the receive stream. When PSLMPAIS is set low, path signal label mismatch events will not assert path AIS.

LOPCONPAIS:

When set high, the LOPCONPAIS bit enables path AIS insertion when loss of pointer concatenation (LOPCON) events are detected in the receive stream. When LOPCONPAIS is set low, loss of pointer concatenation events will not assert path AIS.

PAISCONPAIS:

When set high, the PAISCONPAIS bit enables path AIS insertion when Path AIS concatenation (PAISCON) events are detected in the receive direction. When PAISCONPAIS is set low, Path AIS concatenation events will not assert path AIS.

Reserved:

This reserved bit must be programmed to default value for proper operation.

Register 0x00E: Channel Receive Alarm Control #1

Bit	Type	Function	Default
Bit 7	R/W	CONEN	0
Bit 6	R/W	PTIMEN	0
Bit 5	R/W	PSLMEN	0
Bit 4	R/W	PERDIEN	0
Bit 3	R/W	PRDIEN	0
Bit 2	R/W	PAISEN	0
Bit 1	R/W	LCDEN	0
Bit 0	R/W	LOPEN	0

Register 0x00F: S/UNI-1x155 Receive Alarm Control #2

Bit	Type	Function	Default
Bit 7	R/W	STIMEN	0
Bit 6	R/W	SFBEREN	0
Bit 5	R/W	SDBEREN	0
Bit 4	R/W	LRDIEN	0
Bit 3	R/W	LAISEN	0
Bit 2	R/W	OOFEN	0
Bit 1	R/W	LOFEN	0
Bit 0	R/W	LOSEN	0

LOSEN, LOFEN, OOFEN, LAISEN, LRDIEN, SDBEREN, SFBEREN, STIMEN, LOPEN, LCDEN, PAISEN, PRDIEN, PERDIEN, PSLMEN, PTIMEN, CONEN:

The above enable bits allow the corresponding alarm indications to be reported (ORed) into the channel's RALRM output. When the enable bit is high, the corresponding alarm indication is combined with other alarm indications and output on the channel's RALRM. When the enable bit is low, the corresponding alarm indication does not affect the channel's RALRM output.

Alarm	Description
LOS	Loss of signal
LOF	Loss of frame
OOF	Out of Frame
LAIS	Line Alarm Indication Signal
LRDI	Line Remote Defect Indication
SDBER	Signal Degrade Bit Error Rate
SFBER	Signal Fail Bit Error Rate
STIM	Section Trace Identifier Mismatch
LOP	Loss of Pointer
LCD	Loss of Cell Delineation
PAIS	Path Alarm Indication Signal
PRDI	Path Remote Defect Indication
PERDI	Path Enhanced Remote Defect Indication
PSLM	Path Signal Label Mismatch
PTIM	Path Trace Identifier Mismatch
CON	Pointer Concatenation Violation or Pointer AIS

Register 0x010: RSOP Control/Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	BLKBIP	0
Bit 6	R/W	DDS	0
Bit 5	W	FOOF	X
Bit 4	R/W	ALGO2	0
Bit 3	R/W	BIPEE	0
Bit 2	R/W	LOSE	0
Bit 1	R/W	LOFE	0
Bit 0	R/W	OOFE	0

OOFE:

The OOFE bit is an interrupt enable for the out-of-frame alarm. When OOFE is set to logic one, an interrupt is generated when the out-of-frame alarm changes state.

LOFE:

The LOFE bit is an interrupt enable for the loss of frame alarm. When LOFE is set to logic one, an interrupt is generated when the loss of frame alarm changes state.

LOSE:

The LOSE bit is an interrupt enable for the loss of signal alarm. When LOSE is set to logic one, an interrupt is generated when the loss of signal alarm changes state.

BIPEE:

The BIPEE bit is an interrupt enable for the section BIP-8 errors. When BIPEE is set to logic one, an interrupt is generated when a section BIP-8 error (B1) is detected.

ALGO2:

The ALGO2 bit position selects the framing algorithm used to determine and maintain the frame alignment. When a logic one is written to the ALGO2 bit position, the framer is enabled to use the second of the framing algorithms where only the first A1 framing byte and the first 4 bits of the last A2 framing byte (12 bits total) are examined. This algorithm examines only 12 bits of the framing pattern regardless; all other framing bits are ignored. When a logic zero is written to the ALGO2 bit position, the framer is enabled to use the first of the framing algorithms where all the A1 framing bytes and all the A2 framing bytes are examined.

FOOF:

The FOOF bit controls the framing of the RSOP. When a logic one is written to FOOF, the RSOP is forced out of frame at the next frame boundary. The FOOF bit is a write only bit. Register reads may yield a logic one or a logic zero.

DDS:

The DDS bit is set to logic one to disable the descrambling of the STS-3c/STM-1 stream. When DDS is a logic zero, descrambling is enabled.

BLKBIP:

The BLKBIP bit position enables the accumulating of section BIP word errors. When a logic one is written to the BLKBIP bit position, one or more errors in the BIP-8 byte result in a single error being accumulated in the B1 error counter. When a logic zero is written to the BLKBIP bit position, all errors in the B1 byte are accumulated in the B1 error counter.

Register 0x011: RSOP Status/Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	BIPEI	X
Bit 5	R	LOSI	X
Bit 4	R	LOFI	X
Bit 3	R	OOFI	X
Bit 2	R	LOSV	X
Bit 1	R	LOFV	X
Bit 0	R	OOFV	X

OOFV:

The OOFV bit is read to determine the out-of-frame state of the RSOP. When OOFV is high, the RSOP is out of frame. When OOFV is low, the RSOP is in-frame.

LOFV:

The LOFV bit is read to determine the loss of frame state of the RSOP. When LOFV is high, the RSOP has declared loss of frame.

LOSV:

The LOSV bit is read to determine the loss of signal state of the RSOP. When LOSV is high, the RSOP has declared loss of signal.

OOFI:

The OOFI bit is the out-of-frame interrupt status bit. OOFI is set high when a change in the out-of-frame state occurs. This bit is cleared when this register is read.

LOFI:

The LOFI bit is the loss of frame interrupt status bit. LOFI is set high when a change in the loss of frame state occurs. This bit is cleared when this register is read.

LOSI:

The LOSI bit is the loss of signal interrupt status bit. LOSI is set high when a change in the loss of signal state occurs. This bit is cleared when this register is read.

BIPEI:

The BIPEI bit is the section BIP-8 interrupt status bit. BIPEI is set high when a section layer (B1) bit error is detected. This bit is cleared when this register is read.

Register 0x012: RSOP Section BIP-8 LSB

Bit	Type	Function	Default
Bit 7	R	SBE[7]	X
Bit 6	R	SBE[6]	X
Bit 5	R	SBE[5]	X
Bit 4	R	SBE[4]	X
Bit 3	R	SBE[3]	X
Bit 2	R	SBE[2]	X
Bit 1	R	SBE[1]	X
Bit 0	R	SBE[0]	X

Register 0x013: RSOP Section BIP-8 MSB

Bit	Type	Function	Default
Bit 7	R	SBE[15]	X
Bit 6	R	SBE[14]	X
Bit 5	R	SBE[13]	X
Bit 4	R	SBE[12]	X
Bit 3	R	SBE[11]	X
Bit 2	R	SBE[10]	X
Bit 1	R	SBE[9]	X
Bit 0	R	SBE[8]	X

SBE[15:0]:

Bits SBE[15:0] represent the number of section BIP-8 errors (individual or block) that have been detected since the last time the error count was polled. The error count is polled by writing to either of the RSOP Section BIP-8 Register addresses. Such a write transfers the internally accumulated error count to the Section BIP-8 registers within approximately 7 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that ensures that coincident events are not lost.

The count can also be polled by writing to the S/UNI-1x155 Master Reset and Identity register (0x000). Writing to register address 0x000 loads all counter registers in the channel and APS link.

The count can also be polled by writing to the channel Master Interrupt Status register (0x007). Writing to register 0x007 loads all counter registers in the RSOP, RLOP, RPOP, SPTB, SSTB, RXCP, TXCP, RXFP, and TXFP blocks of the channel.

Register 0x014: TSOP Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	DS	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	LAIS	0

LAIS:

The LAIS bit controls the insertion of line alarm indication signal (AIS). When LAIS is set to logic one, the TSOP inserts AIS into the transmit SONET/SDH stream. Activation or deactivation of line AIS insertion is synchronized to frame boundaries. Line AIS insertion results in all bits of the SONET/SDH frame being set to 1 prior to scrambling except for the section overhead.

DS:

The DS bit is set to logic one to disable the scrambling of the STS-3c/STM-1 stream. When DS is a logic zero, scrambling is enabled.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x015: TSOP Diagnostic

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	DLOS	0
Bit 1	R/W	DBIP8	0
Bit 0	R/W	DFP	0

DFP:

The DFP bit controls the insertion of a single bit error continuously in the most significant bit (bit 1) of the A1 section overhead framing byte. When DFP is set to logic one, the A1 bytes are set to 0x76 instead of 0xF6.

DBIP8:

The DBIP8 bit controls the insertion of bit errors continuously in the section BIP-8 byte (B1). When DBIP8 is set to logic one, the B1 byte is inverted.

DLOS:

The DLOS bit controls the insertion of all zeros in the STS-3c/STM-1 stream. When DLOS is set to logic one, the transmit stream is forced to 0x00.

Register 0x018: RLOP Control/Status

Bit	Type	Function	Default
Bit 7	R/W	BIPWORD	0
Bit 6	R/W	ALLONES	0
Bit 5	R/W	AISDET	0
Bit 4	R/W	LRDIDET	0
Bit 3	R/W	BIPWORDO	0
Bit 2	R/W	FEBEWORD	0
Bit 1	R	LAISV	X
Bit 0	R	LRDIV	X

LRDIV:

The LRDIV bit is read to determine the remote defect indication state of the RLOP. When LRDIV is high, the RLOP has declared line RDI.

LAISV:

The LAISV bit is read to determine the line AIS state of the RLOP. When LAISV is high, the RLOP has declared line AIS.

FEBEWORD:

The FEBEWORD bit controls the accumulation of FEBEs. When FEBEWORD is high, the FEBE event counter is incremented only once per frame whenever one or more FEBE bits occur during that frame. When FEBEWORD is low, the FEBE event counter is incremented for each and every FEBE bit that occurs during that frame (the counter can be incremented up to 24.

BIPWORDO:

The BIPWORDO bit controls the indication of B2 errors reported to the TLOP block for insertion as FEBEs. When BIPWORDO is logic one, the BIP errors are indicated once per frame whenever one or more B2 bit errors occur during that frame. When BIPWORDO is logic zero, BIP errors are indicated once for every B2 bit error that occurs during that frame. The accumulation of B2 error events functions independently and is controlled by the BIPWORD register bit.

LRDIDET:

The LRDIDET bit determines the line RDI alarm detection algorithm. When LRDIDET is set to logic one, line RDI is declared when a 110 binary pattern is detected in bits 6, 7 and 8 of the K2 byte for three consecutive frames. When LRDIDET is set to logic zero, line RDI is declared when a 110 binary pattern is detected in bits 6, 7 and 8 of the K2 byte for five consecutive frames.

AISDET:

The AISDET bit determines the line AIS alarm detection algorithm. When AISDET is set to logic one, line AIS is declared when a 111 binary pattern is detected in bits 6, 7 and 8 of the K2 byte for three consecutive frames. When AISDET is set to logic zero, line AIS is declared when a 111 binary pattern is detected in bits 6, 7 and 8 of the K2 byte for five consecutive frames.

ALLONES:

The ALLONES bit controls automatically forcing the SONET/SDH frame passed to downstream blocks to logical all-ones whenever line AIS is detected. When ALLONES is set to logic one, the SONET/SDH frame is forced to logic one immediately when the line AIS alarm is declared. When line AIS is removed, the downstream data stream is immediately returned to carrying the receive data. When ALLONES is set to logic zero, the downstream data stream always carries the receive data regardless of the line AIS alarm state.

BIPWORD:

The BIPWORD bit controls the accumulation of B2 errors. When BIPWORD is logic one, the B2 error event counter is incremented only once per frame whenever one or more B2 bit errors occur during that frame. When BIPWORD is logic zero, the B2 error event counter is increment for each and every B2 bit error that occurs during that frame.

Register 0x019: RLOP Interrupt Enable/Interrupt Status

Bit	Type	Function	Default
Bit 7	R/W	FEBEE	0
Bit 6	R/W	BIPEE	0
Bit 5	R/W	LAISE	0
Bit 4	R/W	LRDIE	0
Bit 3	R	FEBEI	X
Bit 2	R	BIPEI	X
Bit 1	R	LAISI	X
Bit 0	R	LRDII	X

LRDII:

The LRDII bit is the remote defect indication interrupt status bit. LRDII is set high when a change in the line RDI state occurs. This bit is cleared when this register is read.

LAISI:

The LAISI bit is the line AIS interrupt status bit. LAISI is set high when a change in the line AIS state occurs. This bit is cleared when this register is read.

BIPEI:

The BIPEI bit is the line BIP-24 interrupt status bit. BIPEI is set high when a line layer (B2) bit error is detected. This bit is cleared when this register is read.

FEBEI:

The FEBEI bit is the line far end block error interrupt status bit. FEBEI is set high when a line layer FEBE (M1) is detected. This bit is cleared when this register is read.

LRDIE:

The LRDIE bit is an interrupt enable for the line remote defect indication alarm. When LRDIE is set to logic one, an interrupt is generated when the line RDI state changes.

LAISE:

The LAISE bit is an interrupt enable for line AIS. When LAISE is set to logic one, an interrupt is generated when line AIS changes state.

BIPEE:

The BIPEE bit is an interrupt enable for the line BIP-24 errors. When BIPEE is set to logic one, an interrupt is generated when a line BIP-24 error (B2) is detected.

FEBEE:

The FEBEE bit is an interrupt enable for the line far end block errors. When FEBEE is set to logic one, an interrupt is generated when FEBE (Z2) is detected.

Register 0x01A: RLOP Line BIP-24 LSB

Bit	Type	Function	Default
Bit 7	R	LBE[7]	X
Bit 6	R	LBE[6]	X
Bit 5	R	LBE[5]	X
Bit 4	R	LBE[4]	X
Bit 3	R	LBE[3]	X
Bit 2	R	LBE[2]	X
Bit 1	R	LBE[1]	X
Bit 0	R	LBE[0]	X

Register 0x01B: RLOP Line BIP-24

Bit	Type	Function	Default
Bit 7	R	LBE[15]	X
Bit 6	R	LBE[14]	X
Bit 5	R	LBE[13]	X
Bit 4	R	LBE[12]	X
Bit 3	R	LBE[11]	X
Bit 2	R	LBE[10]	X
Bit 1	R	LBE[9]	X
Bit 0	R	LBE[8]	X

Register 0x01C: RLOP Line BIP-24 MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	LBE[19]	X
Bit 2	R	LBE[18]	X
Bit 1	R	LBE[17]	X
Bit 0	R	LBE[16]	X

LBE[19:0]

Bits LBE[19:0] represent the number of line BIP-24 errors (individual or block) that have been detected since the last time the error count was polled. The error count is polled by writing to any of the RLOP Line BIP-24 Register or Line FEBE Register addresses. Such a write transfers the internally accumulated error count to the Line BIP-24 Registers within approximately 7 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation.

The count can also be polled by writing to the S/UNI-1x155 Master Reset and Identity register (0x000). Writing to register address 0x000 loads all counter registers in the channel and APS link.

The count can also be polled by writing to the channel Master Interrupt Status register (0x007). Writing to register 0x007 loads all counter registers in the RSOP, RLOP, RPOP, SPTB, SSTB, RXCP, TXCP, RXFP, and TXFP blocks of the channel.

Register 0x01D: RLOP Line FEBE LSB

Bit	Type	Function	Default
Bit 7	R	LFE[7]	X
Bit 6	R	LFE[6]	X
Bit 5	R	LFE[5]	X
Bit 4	R	LFE[4]	X
Bit 3	R	LFE[3]	X
Bit 2	R	LFE[2]	X
Bit 1	R	LFE[1]	X
Bit 0	R	LFE[0]	X

Register 0x01E: RLOP Line FEBE

Bit	Type	Function	Default
Bit 7	R	LFE[15]	X
Bit 6	R	LFE[14]	X
Bit 5	R	LFE[13]	X
Bit 4	R	LFE[12]	X
Bit 3	R	LFE[11]	X
Bit 2	R	LFE[10]	X
Bit 1	R	LFE[9]	X
Bit 0	R	LFE[8]	X

Register 0x01F: RLOP Line FEBE MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	LFE[19]	X
Bit 2	R	LFE[18]	X
Bit 1	R	LFE[17]	X
Bit 0	R	LFE[16]	X

LFE[19:0]

Bits LFE[19:0] represent the number of line FEBE errors (individual or block) that have been detected since the last time the error count was polled. The error count is polled by writing to any of the RLOP Line BIP-24 Register or Line FEBE Register addresses. Such a write transfers the internally accumulated error count to the Line FEBE Registers within approximately 7 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation.

The count can also be polled by writing to the S/UNI-1x155 Master Reset and Identity register (0x000). Writing to register address 0x000 loads all counter registers in the channel and APS link

The count can also be polled by writing to the channel Master Interrupt Status register (0x007). Writing to register 0x007 loads all counter registers in the RSOP, RLOP, RPOP, SPTB, SSTB, RXCP, TXCP, RXFP, and TXFP blocks of the channel.

Register 0x020: TLOP Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	APSREG	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	LRDI	0

LRDI:

The LRDI bit controls the insertion of line remote defect indication (LRDI). When LRDI is set to logic one, the TLOP inserts line RDI into the transmit SONET/SDH stream. Line RDI is inserted by transmitting the code 110 in bit positions 6, 7 and 8 of the K2 byte of the STS-3c stream.

APSREG:

The APSREG bit selects the source for the transmit APS channel K1/K2 bytes. When APSREG is a logic zero, 0x0000 is inserted in the transmit APS K1 and K2 bytes. When APSREG is a logic one, the transmit APS channel is inserted from the TLOP Transmit K1 Register and the TLOP Transmit K2 Register.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x021: TLOP Diagnostic

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	DBIP96	0

DBIP96:

The DBIP96 bit controls the insertion of bit errors continuously in the line BIP-24 bytes (B2). When DBIP96 is set to logic one, the B2 bytes are inverted.

Register 0x022: TLOP Transmit K1

Bit	Type	Function	Default
Bit 7	R/W	K1[7]	0
Bit 6	R/W	K1[6]	0
Bit 5	R/W	K1[5]	0
Bit 4	R/W	K1[4]	0
Bit 3	R/W	K1[3]	0
Bit 2	R/W	K1[2]	0
Bit 1	R/W	K1[1]	0
Bit 0	R/W	K1[0]	0

K1[7:0]:

The K1[7:0] bits contain the value inserted in the K1 byte when the APSREG bit in the TLOP Control Register is logic one. K1[7] is the most significant bit corresponding to bit 1, the first bit transmitted. K1[0] is the least significant bit, corresponding to bit 8, the last bit transmitted. The bits in this register are double buffered so that register writes do not need to be synchronized to SONET/SDH frame boundaries. The insertion of a new APS code value is initiated by a write to this register. The contents of this register, and the TLOP Transmit K2 Register are inserted in the SONET/SDH stream starting at the next frame boundary. Successive writes to this register must be spaced at least two frames (250 µs) apart.

Register 0x023: TLOP Transmit K2

Bit	Type	Function	Default
Bit 7	R/W	K2[7]	0
Bit 6	R/W	K2[6]	0
Bit 5	R/W	K2[5]	0
Bit 4	R/W	K2[4]	0
Bit 3	R/W	K2[3]	0
Bit 2	R/W	K2[2]	0
Bit 1	R/W	K2[1]	0
Bit 0	R/W	K2[0]	0

K2[7:0]:

The K2[7:0] bits contain the value inserted in the K2 byte when the APSREG bit in the TLOP Control Register is logic one. K2[7] is the most significant bit corresponding to bit 1, the first bit transmitted. K2[0] is the least significant bit, corresponding to bit 8, the last bit transmitted. The bits in this register are double buffered so that register writes do not need to be synchronized to SONET/SDH frame boundaries. The insertion of a new APS code value is initiated by a write to the TLOP Transmit K1 Register. A coherent APS code value is ensured by writing the desired K2 APS code value to this register before writing the TLOP Transmit K1 Register.

Register 0x024: TLOP Transmit Synchronization Message (S1)

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	TS1[3]	0
Bit 2	R/W	TS1[2]	0
Bit 1	R/W	TS1[1]	0
Bit 0	R/W	TS1[0]	0

TS1[3:0]:

The value written to these bit positions is inserted in the first S1 byte position of the transmit stream. The S1 byte is used to carry synchronization status messages between line terminating network elements. TS1[3] is the most significant bit, corresponding to the first bit transmitted. TS1[0] is the least significant bit, corresponding to the last bit transmitted.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x025: TLOP Transmit J0/Z0

Bit	Type	Function	Default
Bit 7	R/W	J0/Z0[7]	1
Bit 6	R/W	J0/Z0[6]	1
Bit 5	R/W	J0/Z0[5]	0
Bit 4	R/W	J0/Z0[4]	0
Bit 3	R/W	J0/Z0[3]	1
Bit 2	R/W	J0/Z0[2]	1
Bit 1	R/W	J0/Z0[1]	0
Bit 0	R/W	J0/Z0[0]	0

J0/Z0[7:0]:

The value written to this register is inserted into the J0/Z0 byte positions of the transmit stream when enabled using the SDH_J0/Z0 register. J0/Z0[7] is the most significant bit, corresponding to the first bit (bit 1) transmitted. J0/Z0[0] is the least significant bit, corresponding to the last bit (bit 8) transmitted.

Register 0x028: SSTB Control

Bit	Type	Function	Default
Bit 7	R/W	ZEROEN	0
Bit 6	R/W	TIMODE	0
Bit 5	R/W	RTIUIE	0
Bit 4	R/W	RTIMIE	0
Bit 3	R/W	PER5	0
Bit 2	R/W	TNULL	1
Bit 1	R/W	NOSYNC	0
Bit 0	R/W	LEN16	0

This register controls the receive and transmit portions of the SSTB.

LEN16:

The section trace message length bit (LEN16) selects the length of the section trace message to be 16 bytes or 64 bytes. When set high, a 16-byte section trace message is selected. If set low, a 64-byte section trace message is selected.

NOSYNC:

The section trace message synchronization disable bit (NOSYNC) disables the writing of the section trace message into the trace buffer to be synchronized to the content of the message. When LEN16 is set high and NOSYNC is set low, the receive section trace message byte with its most significant bit set will be written to the first location in the buffer. When LEN16 is set low, and NOSYNC is also set low, the byte after the carriage return/linefeed (CR/LF) sequence will be written to the first location in the buffer. When NOSYNC is set high, synchronization is disabled, and the section trace message buffer behaves as a circular buffer.

TNULL:

The transmit null bit (TNULL) controls the insertion of an all-zeros section trace identifier message in the transmit stream. When TNULL is set high, the contents of the transmit buffer is ignored and all-zeros bytes are provided to the TSOP block. When TNULL is set low the contents of the transmit section trace buffer is sent to TSOP for insertion into the J0/Z0 transmit section overhead byte. TNULL should be set high before changing the contents of the trace buffer to avoid sending partial messages.

PER5:

The receive trace identifier persistence bit (PER5) controls the number of times a section trace identifier message must be received unchanged before being accepted. When PER5 is set high, a message is accepted when it is received unchanged five times consecutively. When PER5 is set low, the message is accepted after three identical repetitions.

RTIMIE:

The RTIMIE bit controls the activation of the interrupt output when the comparison between the trace identifier mode 1 accepted identifier message and the expected message changes state. When RTIMIE is a logic one, changes in match state activates the interrupt (INTB) output.

This register is ignored when TIMODE is set high.

RTIUIE:

The RTIUIE bit controls the activation of the interrupt output when, in either trace identifier mode, the receive identifier message changes state. When RTIUIE is a logic one, changes in the received section trace identifier message stable/unstable state will activate the interrupt (INTB) output.

TIMODE:

The trace identifier mode is used to set the mode used for the received trace identifier. Setting TIMODE low sets the trace identifier mode to 1. In this mode, the trace identifier is defined as a regular 16 or 64 byte trace message and persistency is based on the whole message. Receive trace identifier mismatch (RTIM) and unstable (RTIU) alarms are declared on the trace message.

Setting TIMODE high sets the trace identifier mode to 2. In this mode, the trace identifier is defined as a single byte that is monitored for persistency and then errors. A receive trace identifier unstable (RTIU) alarm is declared when one or more errors are detected in three consecutive 16 byte windows.

ZEROEN:

For trace identifier mode 1 only, the zero enable bit (ZEROEN) enables TIM assertion and removal based on an all ZEROs section trace message string. When ZEROEN is set high, all ZEROs section trace message strings are considered when entering and exiting TIM states. When ZEROEN is set low, all ZEROs section trace message strings are ignored.

This register is ignored when in trace identifier mode 2 (controlled by TIMODE).

Register 0x029: SSTB Section Trace Identifier Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	RTIUI	X
Bit 2	R	RTIUV	X
Bit 1	R	RTIMI	X
Bit 0	R	RTIMV	X

This register reports the section trace identifier status of the SSTB.

RTIMV:

When TIMODE is low, the RTIMV bit reports the match/mismatch status of the identifier message framer. RTIMV is a logic one when the accepted identifier message differs from the expected message written by the microprocessor. The accepted message is the last message to have been received 5 consecutive times. RTIMV is a logic zero when the accepted message matches the expected message.

If the accepted message string is all-zeros, the mismatch is not declared unless the ZEROEN register bit is set. This register is invalid when TIMODE is high.

RTIMI:

When TIMODE is low, the RTIMI bit is a logic one when match/mismatch status of the trace identifier framer changes state. This bit is cleared when this register is read. This register is invalid when TIMODE is high.

RTIUV:

The RTIUV bit reports the stable/unstable status of the identifier message framer.

When TIMODE is low, RTIUV is set high when 8 trace messages mismatching against their immediate predecessor message have been received without a persistent message being detected. The unstable counter is incremented on each message that mismatches its predecessor and is cleared on the reception of a persistent message. RTIUV is set high when the unstable counter reaches 8. RTIUV is set low and the unstable counter cleared once a persistent message has been received.

When TIMODE is high, RTIUV is set low during the stable state which is declared after having received the same trace byte for 48 consecutive SONET/SDH frames. The stable byte is declared the accepted byte. RTIUV is set high when mismatches between the accepted byte and the received byte have been detected for three consecutive 16 byte windows. The 16 byte windows do not overlap and start immediately after the 48th persistent byte.

RTIUI:

The RTIUI bit is a logic one when stable/unstable status of the trace identifier framer changes state. When RTIUV changes value, RTIUI is set high. This bit is cleared when this register is read.

Register 0x02A: SSTB Indirect Address Register

Bit	Type	Function	Default
Bit 7	R/W	A[7]	0
Bit 6	R/W	A[6]	0
Bit 5	R/W	A[5]	0
Bit 4	R/W	A[4]	0
Bit 3	R/W	A[3]	0
Bit 2	R/W	A[2]	0
Bit 1	R/W	A[1]	0
Bit 0	R/W	A[0]	0

This register supplies the address used to index into section trace identifier buffers. Writing to this register triggers the indirect read/write access to the trace buffer.

A[7:0]:

The indirect read address bits (A[7:0]) indexes into the path trace identifier buffers. Addresses 0 to 63 reference the transmit message buffer which contains the identifier message to be inserted into the transmit stream.

Addresses 64 to 127 reference the receive accepted message page. A receive message is accepted into this page when it is received unchanged three or five times consecutively as determined by the PER5 bit setting.

Addresses 128 to 191 reference the receive capture page while addresses 192 to 255 reference the receive expected page. The receive capture page contains the identifier bytes extracted from the receive stream. The receive expected page contains the expected trace identifier message down-loaded from the microprocessor.

Register 0x02B: SSTB Indirect Data Register

Bit	Type	Function	Default
Bit 7	R/W	D[7]	0
Bit 6	R/W	D[6]	0
Bit 5	R/W	D[5]	0
Bit 4	R/W	D[4]	0
Bit 3	R/W	D[3]	0
Bit 2	R/W	D[2]	0
Bit 1	R/W	D[1]	0
Bit 0	R/W	D[0]	0

This register contains the data read from the section trace message buffer after a read operation or the data to be written into the buffer before a write operation.

D[7:0]:

The indirect data bits (D[7:0]) reports the data read from a message buffer after an indirect read operation has completed. The data to be written to a buffer must be set up in this register before initiating an indirect write operation.

The current and accepted message pages should be read at least twice and the results of the successive reads compared for consistency. The section trace message buffer keeps overwriting these message pages and consequently the result of a read can be composed of multiple messages.

Register 0x02E: SSTB Indirect Access Trigger Register

Bit	Type	Function	Default
Bit 7	R/W	BUSY	0
Bit 6	R/W	RWB	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

BUSY:

The BUSY bit reports whether a previously initiated indirect read or write to a message buffer has been completed. BUSY is set high upon writing to the SSTB Indirect Address register, and stays high until the initiated access has completed, at which point BUSY is set low. This register should be polled to determine when new data is available in the SSTB Indirect Data register.

RWB:

The access control bit (RWB) selects between an indirect read or write access to the static page of the section trace message buffer. Writing to this register initiates an external microprocessor access to the static page of the section trace message buffer. When RWB is set high, a read access is initiated. The data read can be found in the SSTB Indirect Data register. When RWB is set low, a write access is initiated. The data in the SSTB Indirect Data register will be written to the addressed location in the static page.

Register 0x030 (EXTD=0): RPOP Status/Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6		Unused	X
Bit 5	R	PLOPV	X
Bit 4		Unused	X
Bit 3	R	PAISV	X
Bit 2	R	PRDIV	X
Bit 1	R	NEWPTRI	X
Bit 0	R/W	NEWPTRE	0

NOTE: To facilitate additional register mapping, shadow registers have been added to channel registers 0x30, 0x31 and 0x33. These shadow registers are accessed in the same way as the normal registers.

The EXTD (extend register) bit must be set in register 0x36 to allow switching between accessing the normal registers and the shadow registers.

This register allows the status of path level alarms to be monitored.

NEWPTRE:

The NEWPTRE bit is the interrupt enable for the receive new pointer status. When NEWPTRE is a logic one, an interrupt is generated when the pointer interpreter validates a new pointer.

NEWPTRI:

The NEWPTRI bit is the receive new pointer interrupt status bit. NEWPTRI is a logic one when the pointer interpreter has validated a new pointer value (H1, H2). NEWPTRI is cleared when this register is read.

PRDIV:

The PRDIV bit is read to determine the remote defect indication state. When PRDIV is a logic one, the S/UNI-1x155 has declared path RDI.

PAISV:

The PAISV bit is read to determine the path AIS state. When PAISV is a logic one, the S/UNI-1x155 has declared path AIS.

PLOPV:

The PLOPV bit is read to determine the loss of pointer state. When PLOPV is a logic one, the S/UNI-1x155 has declared LOP.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x030 (EXTD=1): RPOP Status/Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	IINVCNT	0
Bit 5	R/W	PSL5	0
Bit 4	R/W	Reserved	0
Bit 3		Unused	X
Bit 2	R	ERDIV[2]	X
Bit 1	R	ERDIV[1]	X
Bit 0	R/W	ERDIV[0]	X

NOTE: To facilitate additional register mapping, shadow registers have been added to channel registers 0x30, 0x31 and 0x33. These shadow registers are accessed in the same way as the normal registers.

The EXTD (extend register) bit must be set in register 0x36 to allow switching between accessing the normal registers and the shadow registers.

The Status Register is provided at RPOP read address 0, if the extend register (EXTD) bit is set in register 6.

ERDIV[2:0]:

The ERDIV[2:0] bits reflect the current state of the detected enhanced RDI, (filtered G1 bits 5, 6, & 7).

IINVCNT:

When IINVCNT (Intuitive Invalid Pointer Counter) bit is set to 1, if the RPOP pointer interpreter state machine is in the LOP state, a new pointer received 3 consecutive times resets the inv_point count. If this bit is set to 0, the inv_point count will not be reset if pointer interpreter is in the LOP state and a new pointer received 3 consecutive times.

PSL5:

The PSL5 bit controls the filtering of the path signal label byte (C2). When PSL5 is set high, the PSL is updated when the same value is received for 5 consecutive frames. When the PSL5 is set low, the PSL is updated when the same value is received for 3 consecutive frames.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x031 (EXTD=0): RPOP Interrupt Status

Bit	Type	Function	Default
Bit 7	R	PSLI	X
Bit 6		Unused	X
Bit 5	R	LOPI	X
Bit 4		Unused	X
Bit 3	R	PAISI	X
Bit 2	R	PRDII	X
Bit 1	R	BIPEI	X
Bit 0	R	FEBEI	X

NOTE: To facilitate additional register mapping, shadow registers have been added to channel registers 0x30, 0x31 and 0x33. These shadow registers are accessed in the same way as the normal registers.

The EXTD (extend register) bit must be set in register 0x36 to allow switching between accessing the normal registers and the shadow registers.

This register allows identification and acknowledgment of path level alarm and error event interrupts.

FEBEI:

The FEBEI bit is the path FEBE interrupt status bit. FEBEI is a logic one when a FEBE error is detected. This bit is cleared when this register is read.

BIPEI:

The BIPEI bit is the path BIP-8 interrupt status bit. BIPEI is a logic one when a B3 error is detected. This bit is cleared when this register is read.

PRDII:

The PRDII bit is the path remote defect indication interrupt status bit. PRDII is a logic one when a change in the path RDI state or the auxiliary path RDI state occurs. This bit is cleared when this register is read.

PAISI:

The PAISI bit is the path alarm indication signal interrupt status bit. PAISI is a logic one when a change in the path AIS state occurs. This bit is cleared when this register is read.

LOPI:

The LOPI bit is the loss of pointer interrupt status bit. LOPI is a logic one when a change in the LOP state occurs. This bit is cleared when this register is read.

PSLI:

The PSLI bit is the change of path signal label interrupt status bit. PSLI is a logic one when a change is detected in the path signal label register. The current path signal label can be read from the RPOP Path Signal Label register. This bit is cleared when this register is read.

Register 0x031 (EXTD=1): RPOP Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	ERDII	X

NOTE: To facilitate additional register mapping, shadow registers have been added to channel registers 0x30, 0x31 and 0x33. These shadow registers are accessed in the same way as the normal registers.

The EXTD (extend register) bit must be set in register 0x36 to allow switching between accessing the normal registers and the shadow registers.

This register allows identification and acknowledgment of path level alarm and error event interrupts.

ERDII:

The ERDII bit is set high when a change is detected in the received enhanced RDI state. This bit is cleared when the RPOP Interrupt Status register is read.

Register 0x032: RPOP Pointer Interrupt Status

Bit	Type	Function	Default
Bit 7	R	ILLJREQI	X
Bit 6		Unused	X
Bit 5	R	DISCOPAI	X
Bit 4	R	INVNDFI	X
Bit 3	R	ILLPTRI	X
Bit 2	R	NSEI	X
Bit 1	R	PSEI	X
Bit 0	R	NDFI	X

This register allows identification and acknowledgment of pointer event interrupts.

NDFI:

The NDFI bit is set to logic one when the RPOP detects an active NDF event to a valid pointer value. NDFI is cleared when the RPOP Pointer Interrupt Status register is read.

PSEI:

The PSEI bit is set to logic one when the RPOP detects a positive stuff event. PSEI is cleared when the RPOP Pointer Interrupt Status register is read.

NSEI:

The NSEI bit is set to logic one when the RPOP detects a negative stuff event. NSEI is cleared when the RPOP Pointer Interrupt Status register is read.

ILLPTRI:

The ILLPTRI bit is set to logic one when the RPOP detects an illegal pointer event. ILLPTRI is cleared when the RPOP Pointer Interrupt Status register is read.

INVNDFI:

The INVNDFI bit is set to logic one when the RPOP detects an invalid NDF event. INVNDFI is cleared when the RPOP Pointer Interrupt Status register is read.

DISCOPAI:

The DISCOPAI bit is set to logic one when the RPOP detects a discontinuous change of pointer. DISCOPAI is cleared when the RPOP Pointer Interrupt Status register is read.

ILLJREQI:

The ILLJREQI bit is set to logic one when the RPOP detects an illegal pointer justification request event. ILLJREQI is cleared when the RPOP Pointer Interrupt Status register is read.

Register 0x033 (EXTD=0): RPOP Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	PSLE	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	LOPE	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	PAISE	0
Bit 2	R/W	PRDIE	0
Bit 1	R/W	BIPEE	0
Bit 0	R/W	FEBEE	0

NOTE: To facilitate additional register mapping, shadow registers have been added to channel registers 0x30, 0x31 and 0x33. These shadow registers are accessed in the same way as the normal registers.

The EXTD (extend register) bit must be set in register 0x36 to allow switching between accessing the normal registers and the shadow registers.

This register allows interrupt generation to be enabled for path level alarm and error events.

FEBEE:

The FEBEE bit is the interrupt enable for path FEBEs. When FEBEE is a logic one, an interrupt is generated when a path FEBE is detected.

BIPEE:

The BIPEE bit is the interrupt enable for path BIP-8 errors. When BIPEE is a logic one, an interrupt is generated when a B3 error is detected.

PRDIE:

The PRDIE bit is the interrupt enable for path RDI. When PRDIE is a logic one, an interrupt is generated when the path RDI state changes.

PAISE:

The PAISE bit is the interrupt enable for path AIS. When PAISE is a logic one, an interrupt is generated when the path AIS state changes.

LOPE:

The LOPE bit is the interrupt enable for LOP. When LOPE is a logic one, an interrupt is generated when the LOP state changes.

PSLE:

The PSLE bit is the interrupt enable for changes in the received path signal label. When PSLE is a logic one, an interrupt is generated when the received C2 byte changes.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x033 (EXTD=1): RPOP Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	ERDIE	0

NOTE: To facilitate additional register mapping, shadow registers have been added to channel registers 0x30, 0x31 and 0x33. These shadow registers are accessed in the same way as the normal registers.

The EXTD (extend register) bit must be set in register 0x36 to allow switching between accessing the normal registers and the shadow registers.

This register allows interrupt generation to be enabled for path level alarm and error events.

ERDIE:

When ERDIE is a logic one, an interrupt is generated when a path enhanced RDI is detected.

Register 0x034: RPOP Pointer Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	ILLJREQE	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	DISCOPAE	0
Bit 4	R/W	INVNDFE	0
Bit 3	R/W	ILLPTRE	0
Bit 2	R/W	NSEE	0
Bit 1	R/W	PSEE	0
Bit 0	R/W	NDFE	0

This register is used to enable pointer event interrupts.

NDFE:

When a logic one is written to the NDFE interrupt enable bit position, an interrupt is generated when a change in active offset due to the reception of an enabled NDF (NDF_enabled indication) occurs.

PSEE:

When a logic one is written to the PSEE interrupt enable bit position, an interrupt is generated when a positive pointer adjustment event is received.

NSEE:

When a logic one is written to the NSEE interrupt enable bit position, an interrupt is generated when a negative pointer adjustment is received.

ILLPTRE:

When a logic one is written to the ILLPTRE interrupt enable bit position, an interrupt is generated when an illegal pointer is received.

INVNDFE:

When a logic one is written to the INVNDFE interrupt enable bit position, an interrupt is generated when an invalid NDF code is received.

DISCOPAE:

When a logic one is written to the DISCOPAE interrupt enable bit position, an interrupt is generated when a change of pointer alignment event occurs.

ILLJREQE:

When a logic one is written to the ILLJREQE interrupt enable bit position, an interrupt is generated when an illegal pointer justification request is received.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x035: RPOP Pointer LSB

Bit	Type	Function	Default
Bit 7	R	PTR[7]	X
Bit 6	R	PTR[6]	X
Bit 5	R	PTR[5]	X
Bit 4	R	PTR[4]	X
Bit 3	R	PTR[3]	X
Bit 2	R	PTR[2]	X
Bit 1	R	PTR[1]	X
Bit 0	R	PTR[0]	X

Register 0x036: RPOP Pointer MSB

Bit	Type	Function	Default
Bit 7	R/W	NDFPOR	0
Bit 6	R/W	EXTD	0
Bit 5	R/W	RDI10	0
Bit 4		Unused	X
Bit 3	R	S1	X
Bit 2	R	S0	X
Bit 1	R	PTR[9]	X
Bit 0	R	PTR[8]	X

PTR[9:0]:

The PTR[7:0] bits contain the current pointer value as derived from the H1 and H2 bytes. To ensure reading a valid pointer, the NDFI, NSEI and PSEI bits of the RPOP Pointer Interrupt Status register should be read before and after reading this register to ensure that the pointer value did not changed during the register read.

S0, S1:

The S0 and S1 bits contain the two S bits received in the last H1 byte. These bits should be software debounced to ensure the proper values are received.

RDI10:

The RDI10 bit controls the filtering of the remote defect indication and the auxiliary remote defect indication. When RDI10 is set to logic one, the PRDI and ARDI statuses are updated when the same value is received in the corresponding bit of the G1 byte for 10 consecutive frames. When PRDI10 is set to logic zero, the PRDI and ARDI statuses are updated when the same value is received for 5 consecutive frames.

NDFPOR:

The NDFPOR (new data flag pointer outside range) bit allows an NDF counter enable, if the pointer value is outside the range (0-782). If this bit is set high the definition for NDF counter enable is enabled NDF + ss. If this bit is set low the definition for NDF counter enable is enabled NDF + ss + offset in the range of 0 to 782. Note that this bit only allows the NDF counter to count towards LOP when the pointer is out of range and no active offset change will occur.

EXTD:

The EXTD bit extends the registers to facilitate additional mapping. If this bit is set high, the register mapping, for registers 0x30, 0x31 and 0x33, are extended.

Register 0x037: RPOP Path Signal Label

Bit	Type	Function	Default
Bit 7	R	PSL[7]	X
Bit 6	R	PSL[6]	X
Bit 5	R	PSL[5]	X
Bit 4	R	PSL[4]	X
Bit 3	R	PSL[3]	X
Bit 2	R	PSL[2]	X
Bit 1	R	PSL[1]	X
Bit 0	R	PSL[0]	X

PSL[7:0]:

The PSL[7:0] bits contain the path signal label byte (C2). The value in this register is updated to a new path signal label value if the same new value is observed for three or five consecutive frames, depending on the status of the PSL5 bit.

Register 0x038: RPOP Path BIP-8 LSB

Bit	Type	Function	Default
Bit 7	R	PBE[7]	X
Bit 6	R	PBE[6]	X
Bit 5	R	PBE[5]	X
Bit 4	R	PBE[4]	X
Bit 3	R	PBE[3]	X
Bit 2	R	PBE[2]	X
Bit 1	R	PBE[1]	X
Bit 0	R	PBE[0]	X

Register 0x039: RPOP Path BIP-8 MSB

Bit	Type	Function	Default
Bit 7	R	PBE[15]	X
Bit 6	R	PBE[14]	X
Bit 5	R	PBE[13]	X
Bit 4	R	PBE[12]	X
Bit 3	R	PBE[11]	X
Bit 2	R	PBE[10]	X
Bit 1	R	PBE[9]	X
Bit 0	R	PBE[8]	X

These registers allow path BIP-8 errors to be accumulated.

PBE[15:0]:

PBE[15:0] represent the number of B3 errors (individual or block) that have been detected since the last time the error count was polled. The error count is polled by writing to either of the RPOP Path BIP-8 Register addresses or to either of the RPOP Path FEBE Register addresses. Such a write transfers the internally accumulated error count to the Path BIP-8 registers within a maximum of 7 μs and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that ensures that coincident events are not lost.

The count can also be polled by writing to the S/UNI-1x155 Master Reset and Identity register (0x000). Writing to register address 0x000 loads all counter registers in the channel and APS link.

The count can also be polled by writing to the channel Master Interrupt Status register (0x007). Writing to register 0x007 loads all counter registers in the RSOP, RLOP, RPOP, SPTB, SSTB, RXCP, TXCP, RXFP, and TXFP blocks of the channel.

Register 0x03A: RPOP Path FEBE LSB

Bit	Type	Function	Default
Bit 7	R	PFE[7]	X
Bit 6	R	PFE[6]	X
Bit 5	R	PFE[5]	X
Bit 4	R	PFE[4]	X
Bit 3	R	PFE[3]	X
Bit 2	R	PFE[2]	X
Bit 1	R	PFE[1]	X
Bit 0	R	PFE[0]	X

Register 0x03B: RPOP Path FEBE MSB

Bit	Type	Function	Default
Bit 7	R	PFE[15]	X
Bit 6	R	PFE[14]	X
Bit 5	R	PFE[13]	X
Bit 4	R	PFE[12]	X
Bit 3	R	PFE[11]	X
Bit 2	R	PFE[10]	X
Bit 1	R	PFE[9]	X
Bit 0	R	PFE[8]	X

These registers allow path FEBEs to be accumulated.

PFE[15:0]:

Bits PFE[15:0] represent the number of path FEBE errors (individual or block) that have been detected since the last time the error count was polled. The error count is polled by writing to either of the RPOP Path BIP-8 Register addresses or to either of the RPOP Path FEBE Register addresses. Such a write transfers the internally accumulated error count to the Path FEBE Registers within approximately 7 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that ensures that coincident events are not lost.

The count can also be polled by writing to the S/UNI-1x155 Master Reset and Identity register (0x000). Writing to register address 0x000 loads all counter registers in the channel and APS link.

The count can also be polled by writing to the channel Master Interrupt Status register (0x007). Writing to register 0x007 loads all counter registers in the RSOP, RLOP, RPOP, SPTB, SSTB, RXCP, TXCP, RXFP, and TXFP blocks of the channel.

Register 0x03C: RPOP RDI

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	BLKFEBE	0
Bit 3		Unused	X
Bit 2	R/W	Reserved	0
Bit 1	R/W	ARDIE	0
Bit 0	R	ARDIV	X

ARDIV:

The auxiliary RDI bit (ARDIV) reports the current state of the path auxiliary RDI within the receive path overhead processor.

ARDIE:

When a logic one is written to the ARDIE interrupt enable bit position, an interrupt is generated when a change in the path auxiliary RDI state occurs. This interrupt is indicated by the PRDII bit (Register 0x031 (EXTD=0); RPOP Interrupt Status, Bit 2).

BLKFEBE:

When set high, the block FEBE bit (BLKFEBE) causes path FEBE errors to be reported and accumulated on a block basis. A single path FEBE error is accumulated for a block if the received FEBE code for that block is between 1 and 8 inclusive. When BLKFEBE is set low, path FEBE errors are accumulated on a error basis.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x03D: RPOP Ring Control

Bit	Type	Function	Default
Bit 7	R/W	SOS	0
Bit 6	R/W	ENSS	0
Bit 5	R/W	BLKBIP	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	BLKBIPO	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

BLKBIPO:

When set high, the block BIP-8 output bit (BLKBIPO) indicates that path BIP-8 errors are to be reported on a block basis to the transmit path overhead processor (TPOP) block. A single path BIP error is reported to the return transmit path overhead processor if any of the path BIP-8 results indicates a mismatch. When BLKBIP is set low, BIP-8 errors are reported on a bit basis.

BLKBIP:

When set high, the block BIP-8 bit (BLKBIP) indicates that path BIP-8 errors are to be accumulated on a block basis. A single BIP error is accumulated if any of the BIP-8 results indicates a mismatch. When BLKBIP is set low, BIP-8 errors are accumulated on a bit basis.

ENSS:

The enable size bit (ENSS) controls whether the SS bits in the payload pointer are used to determine offset changes in the pointer interpreter state machine. When a logic one is written to this bit, an incorrect SS bit pattern (i.e., not equal to 10) will prevent RPOP from issuing NDF_enable, inc_ind, new_point and dec_ind indications. When a logic zero is written to this bit, the received SS bits do not affect active offset change events.

SOS:

The stuff opportunity spacing control bit (SOS) controls the spacing between consecutive pointer justification events on the receive stream. When a logic one is written to this bit, the definition of inc_ind and dec_ind indications includes the requirement that active offset changes have occurred a least three frame ago. When a logic zero is written to this bit, pointer justification indications in the receive stream are followed without regard to the proximity of previous active offset changes.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x040: TPOP Control/Diagnostic

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	EPRDIEN	0
Bit 5	R/W	EPRDISRC	0
Bit 4	R/W	PERSIST	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	DBIP8	0
Bit 0	R/W	PAIS	0

For more details refer to the Operation Section of this document.

PAIS:

The PAIS bit controls the insertion of STS path alarm indication signal. When a logic one is written to this bit position, the complete SPE, and the pointer bytes (H1, H2, and H3) are overwritten with the all-ones pattern. When a logic zero is written to this bit position, the pointer bytes and the SPE are processed normally.

DBIP8:

The DBIP8 bit controls the insertion of bit errors continuously in the B3 byte. When DBIP8 is a logic one, the B3 byte is inverted.

EPRDISRC:

The enhanced path receive defect indication alarm source bit (EPRDISRC) controls the source of RDI input to be inserted onto the G1 byte. See the description in register 0x049 for more information on the operation of this register.

EPRDIEN

The enhanced path receive defect indication alarm enable bit (EPRDIEN) controls the use of 3-bit enhanced RDI mode. See the description in register 0x049 for more information on the operation of this register.

PERSIST

The path far end receive failure alarm persistence bit (PERSIST) controls the persistence of the RDI asserted into the transmit stream. When PERSIST is a logic one, the RDI code inserted into the transmit stream as a result of consequential actions is asserted for a minimum of 20 frames in non-enhanced RDI mode, or the last valid RDI code before an idle code (idle codes are when bits 5,6,7 are 000, 001, or 011) is asserted for 20 frames in enhanced RDI mode. When PERSIST is logic zero, the transmit RDI code changes immediately based on received alarm conditions.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x041: TPOP Pointer Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	FTPTR	0
Bit 5	R/W	SOS	0
Bit 4	R/W	PLD	0
Bit 3	R/W	NDF	0
Bit 2	R/W	NSE	0
Bit 1	R/W	PSE	0
Bit 0	R/W	Reserved	0

This register allows control over the transmitted payload pointer for diagnostic purposes.

PSE:

The PSE bit controls the insertion of positive pointer movements. A zero to one transition on this bit enables the insertion of a single positive pointer justification in the outgoing stream. This register bit is automatically cleared when the pointer movement is inserted.

NSE:

The NSE bit controls the insertion of negative pointer movements. A zero to one transition on this bit enables the insertion of a single negative pointer justification in the outgoing stream. This register bit is automatically cleared when the pointer movement is inserted.

NOTE:

NDF:

The NDF bit controls the insertion of new data flags in the inserted payload pointer. When a logic one is written to this bit position, the pattern contained in the NDF[3:0] bit positions in the TPOP Arbitrary Pointer MSB Register is inserted continuously in the payload pointer. When a logic zero is written to this bit position, the normal pattern (0110) is inserted in the payload pointer.

PLD:

The PLD bit controls the loading of the pointer value contained in the TPOP Arbitrary Pointer Registers. Normally the TPOP Arbitrary Pointer Registers are written to set up the arbitrary new pointer value, the S-bit values, and the NDF pattern. A logic one is then written to this bit position to load the new pointer value. The new data flag bit positions are set to the programmed NDF pattern for the first frame; subsequent frames have the new data flag bit positions set to the normal pattern (0110) unless the NDF bit described above is set to a logic one.

Note: When loading an out of range pointer (that is a pointer with a value greater than 782), the TPOP continues to operate with timing based on the last valid pointer value. The out of range pointer value will of course be inserted in the STS-3c/STM-1 stream. Although a valid SPE will continue to be generated, it is unlikely to be extracted by downstream circuitry, which should be in a loss of pointer state.

This bit is automatically cleared after the new payload pointer has been loaded.

SOS:

The SOS bit controls the stuff opportunity spacing between consecutive SPE positive or negative stuff events. When SOS is a logic zero, stuff events may be generated every frame as controlled by the PSE and NSE register bits described above. When SOS is a logic one, stuff events may be generated at a maximum rate of once every four frames.

FTPTR:

The force transmit pointer bit (FTPTR) enables the insertion of the pointer value contained in the Arbitrary Pointer Registers into the SONET/SDH transmit serial stream for diagnostic purposes. This allows the ATM/POS payload mapping circuitry to continue functioning normally and a valid SPE to continue to be generated, although it is unlikely to be extracted by downstream circuitry as the downstream pointer processor should be in a loss of pointer state.

If FTPTR is set to logic one, the APTR[9:0] bits of the Arbitrary Pointer Registers are inserted into the H1 and H2 bytes of the transmit stream. At least one corrupted pointer is guaranteed to be sent. If FTPTR is a logic zero, a valid pointer is inserted.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x043: TPOP Current Pointer LSB

Bit	Type	Function	Default
Bit 7	R	CPTR[7]	X
Bit 6	R	CPTR[6]	X
Bit 5	R	CPTR[5]	X
Bit 4	R	CPTR[4]	X
Bit 3	R	CPTR[3]	X
Bit 2	R	CPTR[2]	X
Bit 1	R	CPTR[1]	X
Bit 0	R	CPTR[0]	X

Register 0x044: TPOP Current Pointer MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	CPTR[9]	X
Bit 0	R	CPTR[8]	X

CPTR[9:0]:

The CPTR[9:0] bits reflect the value of the current payload pointer being inserted in the outgoing stream. The value may be changed by loading a new pointer value using the TPOP Arbitrary Pointer LSB and MSB Registers, or by inserting positive and negative pointer movements using the PSE and NSE register bits.

It is recommended the CPTR[9:0] value be software debounced to ensure a correct value is received.

Register 0x045: TPOP Arbitrary Pointer LSB

Bit	Type	Function	Default
Bit 7	R/W	APTR[7]	0
Bit 6	R/W	APTR[6]	0
Bit 5	R/W	APTR[5]	0
Bit 4	R/W	APTR[4]	0
Bit 3	R/W	APTR[3]	0
Bit 2	R/W	APTR[2]	0
Bit 1	R/W	APTR[1]	0
Bit 0	R/W	APTR[0]	0

This register allows an arbitrary pointer to be inserted for diagnostic purposes.

APTR[7:0]:

The APTR[7:0] bits, along with the APTR[9:8] bits in the TPOP Arbitrary Pointer MSB Register are used to set an arbitrary payload pointer value. The arbitrary pointer value is inserted in the outgoing stream by writing a logic one to the PLD bit in the TPOP Pointer Control Register.

If the FTPTR bit in the TPOP Pointer Control register is a logic one, the current APTR[9:0] value is inserted into the payload pointer bytes (H1 and H2) in the transmit stream.

Register 0x046: TPOP Arbitrary Pointer MSB

Bit	Type	Function	Default
Bit 7	R/W	NDF[3]	1
Bit 6	R/W	NDF[2]	0
Bit 5	R/W	NDF[1]	0
Bit 4	R/W	NDF[0]	1
Bit 3	R/W	S[1]	1
Bit 2	R/W	S[0]	0
Bit 1	R/W	APTR[9]	0
Bit 0	R/W	APTR[8]	0

This register allows an arbitrary pointer to be inserted for diagnostic purposes.

APTR[9:8]:

The APTR[9:8] bits, along with the APTR[7:0] bits in the TPOP Arbitrary Pointer LSB Register are used to set an arbitrary payload pointer value. The arbitrary pointer value is inserted in the outgoing stream by writing a logic one to the PLD bit in the TPOP Pointer Control Register.

If the FTPTR bit in the TPOP Pointer Control register is a logic one, the current APTR[9:0] value is inserted into the payload pointer bytes (H1 and H2) in the transmit stream.

S[1:0]:

The S[1:0] bits contain the value inserted in the S[1:0] bit positions (also referred to as the unused bits) in the payload pointer. These bits are continuously inserted into the transmit stream.

NDF[3:0]:

The NDF[3:0] bits contain the value inserted in the NDF bit positions when an arbitrary new payload pointer value is inserted (using the PLD bit in the TPOP Pointer Control Register) or when new data flag generation is enabled using the NDF bit in the TPOP Pointer Control Register.

Register 0x047: TPOP Path Trace

Bit	Type	Function	Default
Bit 7	R/W	J1[7]	0
Bit 6	R/W	J1[6]	0
Bit 5	R/W	J1[5]	0
Bit 4	R/W	J1[4]	0
Bit 3	R/W	J1[3]	0
Bit 2	R/W	J1[2]	0
Bit 1	R/W	J1[1]	0
Bit 0	R/W	J1[0]	0

This register allows control over the path trace byte.

J1[7:0]:

The J1[7:0] bits are inserted in the J1 byte position in the transmit stream.

Register 0x048: TPOP Path Signal Label

Bit	Type	Function	Default
Bit 7	R/W	C2[7]	0
Bit 6	R/W	C2[6]	0
Bit 5	R/W	C2[5]	0
Bit 4	R/W	C2[4]	0
Bit 3	R/W	C2[3]	0
Bit 2	R/W	C2[2]	0
Bit 1	R/W	C2[1]	0
Bit 0	R/W	C2[0]	1

This register allows control over the path signal label. Upon reset the register defaults to 0x01, which signifies an equipped unspecific payload.

C2[7:0]:

The C2[7:0] bits are inserted in the C2 byte position in the transmit stream.

C2 should be reprogrammed with the value 0x13 when transmitting ATM payload data.

C2 should be reprogrammed with the value 0x16 when transmitting scrambled packet over SONET payload data.

C2 may be reprogrammed with the value 0xCF when transmitting unscrambled packet over SONET payload data. However, POS scrambling in the TXFP block must be turned off.

Register 0x049: TPOP Path Status

Bit	Type	Function	Default
Bit 7	R/W	FEBE[3]	0
Bit 6	R/W	FEBE[2]	0
Bit 5	R/W	FEBE[1]	0
Bit 4	R/W	FEBE[0]	0
Bit 3	R/W	PRDI	0
Bit 2	R/W	EPRDI6	0
Bit 1	R/W	EPRDI7	0
Bit 0	R/W	G1[0]	0

This register allows control over the path status byte. For more details refer to the Operation Section of this document.

G1[0]:

The G1[0] bit is inserted in bit 0 the Path Status Byte G1. This bit is currently undefined by SONET/SDH standards and should be set to 0.

PRDI, EPRDI6, EPRDI7]:

The PRDI, EPRDI6 and EPRDI7 bits are inserted in bits 5, 6 and 7 of the Path Status Byte G1 respectively. The following describes the operation of these registers based on the EPRDIEN and EPRDISRC configuration bits in register offset 0x40.

The value specified in the table by "AUTORDI" and "AUTOERDI" are the automatic path RDI and enhanced PRDI responses as configured in the Auto RDI and Auto Enhanced RDI configuration registers (offset 0x09, 0x0A and 0x0B). The path RDI response is enabled by the channel AUTOPRDI bit in register offset 0x05.

When auto path alarm operation is desired, the APRDI, PRDI and G1[1:0] registers should be set low.

EPRDIEN	EPRDISRC	G1[5]	G1[6]	G1[7]
0	X	AUTORDI + PRDI	EPRDI6	EPRDI7
1	0	PRDI	EPRDI6	EPRDI7
1	1	AUTOERDI	AUTOERDI	AUTOERDI

FEBE[3:0]:

The FEBE[3:0] bits are inserted in the FEBE bit positions in the path status byte. The value contained in FEBE[3:0] is cleared after being inserted in the path status byte. Any non-zero FEBE[3:0] value overwrites the value that would normally have been inserted based on the number of FEBEs accumulated on primary input FEBE during the last frame. When reading this register, a non-zero value in these bit positions indicates that the insertion of this value is still pending.

Register 0x04E: TPOP Concatenation LSB

Bit	Type	Function	Default
Bit 7	R/W	CONCAT[7]	1
Bit 6	R/W	CONCAT[6]	1
Bit 5	R/W	CONCAT[5]	1
Bit 4	R/W	CONCAT[4]	1
Bit 3	R/W	CONCAT[3]	1
Bit 2	R/W	CONCAT[2]	1
Bit 1	R/W	CONCAT[1]	1
Bit 0	R/W	CONCAT[0]	1

Register 0x04F: TPOP Concatenation MSB

Bit	Type	Function	Default
Bit 7	R/W	CONCAT[15]	1
Bit 6	R/W	CONCAT[14]	0
Bit 5	R/W	CONCAT[13]	0
Bit 4	R/W	CONCAT[12]	1
Bit 3	R/W	CONCAT[11]	0
Bit 2	R/W	CONCAT[10]	0
Bit 1	R/W	CONCAT[9]	1
Bit 0	R/W	CONCAT[8]	1

These registers allow control over the concatenation indication values transmitted in SONET/SDH pointers.

CONCAT[15:0]:

The CONCAT[15:0] bits control the value inserted in the some of the H1 and H2 byte positions when transmitting an STS-3c or STM-1 stream. The value written to CONCAT[15:8] is inserted in the H1 byte position of STS-1 #2 and STS-1 #3 in the concatenated stream. The value written to CONCAT[7:0] is inserted in the H2 byte position of STS-1 #2 and STS-1 #3 in the concatenated stream. The default values represent the normal concatenation indication (all ones in the pointer bits, zeros in the unused bits, and NDF indication).

Register 0x050: SPTB Control

Bit	Type	Function	Default
Bit 7	R/W	ZEROEN	0
Bit 6	R/W	TIMODE	0
Bit 5	R/W	RTIUIE	0
Bit 4	R/W	RTIMIE	0
Bit 3	R/W	PER5	0
Bit 2	R/W	TNULL	1
Bit 1	R/W	NOSYNC	0
Bit 0	R/W	LEN16	0

This register controls the receive and transmit portions of the SPTB.

LEN16:

The LEN16 bit selects the length of the path trace message to be 16 bytes or 64 bytes. When LEN16 is a logic one, a 16 byte path trace message is selected. When LEN16 is a logic zero, a 64 byte path trace message is selected.

NOSYNC:

The NOSYNC bit disables the writing of the path trace message into the trace buffer to be synchronized to the content of the message. When LEN16 is a logic one and NOSYNC is a logic zero, the receive path trace message byte with its most significant bit set will be written to the first location in the buffer. When LEN16 and NOSYNC are logic zero, the byte after the carriage return/linefeed (CR/LF) sequence will be written to the first location in the buffer. When NOSYNC is a logic one, synchronization is disabled, and the path trace message buffer behaves as a circular buffer.

TNULL:

The TNULL bit controls the insertion of an all-zero path trace identifier message in the transmit stream. When TNULL is a logic one, the contents of the transmit buffer is ignored and all-zeros bytes are inserted. When TNULL is a logic zero, the contents of the transmit path trace buffer is sent to TPOP for insertion into the J1 transmit path overhead byte. TNULL should be set high before changing the contents of the trace buffer to avoid sending partial messages.

PER5:

The PER5 bit controls the number of times a path trace identifier message must be received unchanged before being accepted. When PER5 is a logic one, a message is accepted when it is received unchanged five times consecutively. When PER5 is a logic zero, the message is accepted after three identical repetitions.

RTIMIE:

The RTIMIE bit controls the activation of the interrupt output when the comparison between the trace identifier mode 1 accepted identifier message and the expected message changes state. When RTIMIE is a logic one, changes in match state activates the interrupt (INTB) output.

This register is ignored when TIMODE is high.

RTIUIE:

The RTIUIE bit controls the activation of the interrupt output when the receive identifier message changes state. When RTIUIE is a logic one, changes in the received path trace identifier message stable/unstable state will activate the interrupt output.

TIMODE:

The trace identifier mode is used to set the mode used for the received trace identifier. Setting TIMODE low sets the trace identifier mode to 1. In this mode, the trace identifier is defined as a regular 16 or 64 byte trace message and persistency is based on the whole message. Receive trace identifier mismatch (RTIM) and unstable (RTIU) alarms are declared on the trace message.

Setting TIMODE high sets the trace identifier mode to 2. In this mode, the trace identifier is defined as a single byte that is monitored for persistency and then errors. A receive trace identifier unstable (RTIU) alarm is declared when one or more errors are detected in three consecutive 16 byte windows.

ZEROEN:

When TIMODE is low, the zero enable bit (ZEROEN) enables TIM assertion and removal based on an all ZEROs path trace message string. When ZEROEN is set high, all ZEROs path trace message strings are considered when entering and exiting TIM states. When ZEROEN is set low, all ZEROs path trace message strings are ignored.

This register is ignored when TIMODE is high.

Register 0x051: SPTB Path Trace Identifier Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	UNEQI	X
Bit 4	R	UNEQV	X
Bit 3	R	RTIUI	X
Bit 2	R	RTIUV	X
Bit 1	R	RTIMI	X
Bit 0	R	RTIMV	X

This register reports the path trace identifier status of the SPTB.

RTIMV:

When TIMODE is low, the RTIMV bit reports the match/mismatch status of the identifier message framer. RTIMV is a logic one when the accepted identifier message differs from the expected message written by the microprocessor. The accepted message is the last message to have been received 5 consecutive times. RTIMV is a logic zero when the accepted message matches the expected message.

If the accepted message string is all-zeros, the mismatch is not declared unless the ZEROEN register bit is set. This register is invalid when TIMODE is high.

RTIMI:

When TIMODE is low, the RTIMI bit is a logic one when match/mismatch status of the trace identifier framer changes state. This bit is cleared when this register is read. This register is invalid when TIMODE is high.

RTIUV:

The RTIUV bit reports the stable/unstable status of the identifier message framer.

When TIMODE is low, RTIUV is set high when 8 trace messages mismatching against their immediate predecessor message have been received without a persistent message being detected. The unstable counter is incremented on each message that mismatches its predecessor and is cleared on the reception of a persistent message. RTIUV is set high when the unstable counter reaches 8. RTIUV is set low and the unstable counter cleared once a persistent message has been received.

When TIMODE is high, RTIUV is set low during the stable state which is declared after having received the same trace byte for 48 consecutive SONET/SDH frames. The stable byte is declared the accepted byte. RTIUV is set high when mismatches between the accepted byte and the received byte have been detected for three consecutive 16 byte windows. The 16 byte windows do not overlap and start immediately after the 48th persistent byte.

RTIUI:

The RTIUI bit is a logic one when stable/unstable status of the trace identifier framer changes state. When RTIUV changes value, RTIUI is set high. This bit is cleared when this register is read.

UNEQV:

The unequipped value status bit (UNEQV) indicates the equip status of the path signal label. The functionality of this register is controlled by the PSLMODE register.

When PSLMODE is set low, UNEQV is set high when the accepted path signal label indicates that the path connection is unequipped. UNEQV is set low when the accepted path signal label indicates the path connection is not unequipped.

When PSLMODE is set high, UNEQV is set high upon the reception of five consecutive frames with an unequipped (0x00) label. The bit is set low when five consecutive frames are received with a label other than the unequipped label. The five consecutive labels needed to lower the alarm do not need to be the same. The assertion of UNEQV will automatically prevent a path signal label mismatch alarm.

UNEQI:

The UNEQI bit is a logic one when unequipped status of the trace identifier framer changes state. When UNEQV changes value, UNEQI is set high. This bit is cleared when this register is read.

Register 0x052: SPTB Indirect Address Register

Bit	Type	Function	Default
Bit 7	R/W	A[7]	0
Bit 6	R/W	A[6]	0
Bit 5	R/W	A[5]	0
Bit 4	R/W	A[4]	0
Bit 3	R/W	A[3]	0
Bit 2	R/W	A[2]	0
Bit 1	R/W	A[1]	0
Bit 0	R/W	A[0]	0

This register supplies the address used to index into path trace identifier buffers. Writing to this register triggers the indirect read/write access to the trace buffer.

A[7:0]:

The indirect read address bits (A[7:0]) indexes into the path trace identifier buffers. Addresses 0 to 63 reference the transmit message buffer which contains the identifier message to be inserted into the transmit stream.

Addresses 64 to 127 reference the receive accepted message page. A receive message is accepted into this page when it is received unchanged three or five times consecutively as determined by the PER5 bit setting.

Addresses 128 to 191 reference the receive capture page while addresses 192 to 255 reference the receive expected page. The receive capture page contains the identifier bytes extracted from the receive stream. The receive expected page contains the expected trace identifier message down-loaded from the microprocessor.

Register 0x053: SPTB Indirect Data Register

Bit	Type	Function	Default
Bit 7	R/W	D[7]	0
Bit 6	R/W	D[6]	0
Bit 5	R/W	D[5]	0
Bit 4	R/W	D[4]	0
Bit 3	R/W	D[3]	0
Bit 2	R/W	D[2]	0
Bit 1	R/W	D[1]	0
Bit 0	R/W	D[0]	0

This register contains the data read from the path trace message buffer after a read operation or the data to be written into the buffer before a write operation.

D[7:0]:

The indirect data bits (D[7:0]) contain the data read from either the transmit or receive path trace buffer after an indirect read operation is completed. The data that is written to a buffer is set up in this register before initiating the indirect write operation.

The current and accepted message pages should be read at least twice and the results of the successive reads compared for consistency. The section trace message buffer keeps overwriting these message pages and consequently the result of a read can be composed of multiple messages.

Register 0x054: SPTB Expected Path Signal Label

Bit	Type	Function	Default
Bit 7	R/W	EPSL[7]	0
Bit 6	R/W	EPSL[6]	0
Bit 5	R/W	EPSL[5]	0
Bit 4	R/W	EPSL[4]	0
Bit 3	R/W	EPSL[3]	0
Bit 2	R/W	EPSL[2]	0
Bit 1	R/W	EPSL[1]	0
Bit 0	R/W	EPSL[0]	0

EPSL[7:0]:

The EPSL[7:0] bits contain the expected path signal label byte (C2). EPSL[7:0] is compared with the C2 byte extracted from the receive stream.

When PSLMODE is low, EPSL[7:0] is compared with the accepted path signal label extracted from the receive stream. A path signal label mismatch (PSLM) is declared if the accepted PSL differs from the expected PSL. A path signal label match or mismatch is declared based upon the following table:

Expect	Receive	Action Declared
00	00	Match
00	01	Mismatch
00	XX	Mismatch
01	00	Mismatch
01	01	Match
01	XX	Match
XX	00	Mismatch
XX	01	Match
XX	XX	Match
XX	YY	Mismatch

When PSLMODE is high, EPSL[7:0] is compared with the received C2 bytes extracted from the receive stream. A path signal label mismatch (PSLM) is declared if 5 consecutively received C2 bytes (other than 0x00) differ from the expected PSL. A path signal label match or mismatch is declared based upon the following table:

Expect	Receive	Action Declared
00	00	Unequipped
00	01	Mismatch
00	XX	Mismatch
01	00	Unequipped
01	01	Match

Expect	Receive	Action Declared
01	XX	Match
XX	00	Unequipped
XX	01	Match
XX	XX	Match
XX	YY	Mismatch

EPSL[7:0] should be reprogrammed with the value 0x13 when receiving ATM payload data.

EPSL[7:0] should be reprogrammed with the value 0x16 when receiving scrambled packet over SONET payload data.

EPSL[7:0] may be reprogrammed with the value 0xCF when receiving unscrambled packet over SONET payload data. However, POS scrambling in the RXFP block must be turned off.

Register 0x055: SPTB Path Signal Label Status

Bit	Type	Function	Default
Bit 7	R/W	RPSLUIE	0
Bit 6	R/W	RPSLMIE	0
Bit 5	R/W	UNEQIE	0
Bit 4	R/W	PSLMODE	0
Bit 3	R	RPSLUI	X
Bit 2	R	RPSLUV	X
Bit 1	R	RPSLMI	X
Bit 0	R	RPSLMV	X

RPSLMV:

The RPSLMV bit reports the match/mismatch status between the expected and the accepted path signal label.

When PSLMODE is low, RPSLMV is a logic one when the accepted PSL results in a mismatch with EPSL[7:0]. RPSLMV is a logic zero when the accepted PSL results in a match with the expected PSL.

When PSLMODE is high, PSLMV is a logic one when the received PSL differs from EPSL[7:0]. PSLMV is a logic zero when the accepted PSL matches the expected PSL.

RPSLMI:

The RPSLMI bit is a logic when the match/mismatch status between the accepted and the expected path signal label changes state. This bit is cleared when this register is read.

RPSLUV:

The RPSLUV reports the stable/unstable status of the path signal label in the receive stream. RPSLUV is a logic one when the current received C2 byte differs from the previous C2 byte for five consecutive frames. RPSLUV is a logic zero when the same PSL code is received for five consecutive frames.

RPSLUI:

The RPSLUI bit is a logic one when the stable/unstable status of the path signal label changes state. This bit is cleared when this register is read.

PSLMODE:

The PSL Mode is used to control the match/mismatch status between the expected PSL, the received PSL and the accepted PSL. Setting PSLMODE low causes the expected PSL to be compared with the accepted PSL. Set PSLMODE high causes the expected PSL to be compared to the received PSL.

UNEQIE:

The UNEQIE bit is the interrupt enable for the path signal label unequipped status. When UNEQIE is a logic one, changes in the unequipped state generate an interrupt.

RPSLMIE:

The RPSLMIE bit is the interrupt enable for the path signal label match/mismatch status. When RPSLMIE is a logic one, changes in the match state generate an interrupt.

RPSLUIE:

The RPSLUIE bit is the interrupt enable for the path signal label stable/unstable status. When RPSLUIE is a logic one, changes in the stable/unstable state generate an interrupt.

Register 0x056: SPTB Indirect Access Trigger Register

Bit	Type	Function	Default
Bit 7	R/W	BUSY	0
Bit 6	R/W	RWB	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

BUSY:

The BUSY bit reports whether a previously initiated indirect read or write to a message buffer has been completed. BUSY is set to a logic one immediately upon writing to the SPTB Indirect Address register, and stays high until the initiated access is completed. This register should be polled to determine when new data is available in the SPTB Indirect Data register.

RWB:

The access control bit (RWB) selects between an indirect read or write access to the selected path trace buffer (receive or transmit as determined by the RRAMACC bit). Writing to this register initiates an access to the selected path trace buffer. When RWB is a logic one, a read access is initiated. The addressed location's contents are placed in the SPTB Indirect Data register. When RWB is a logic zero, a write access is initiated. The data in the SPTB Indirect Data register is written to the addressed location in the selected buffer.

Register 0x058: DCRU Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	RUN	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

RUN:

The DLL lock status register bit RUN indicates the DCRU has found an initial delay line lock. When the DCRU is attempting to recover the incoming serial stream, RUN is set high. The RUN register bit is cleared only by a system reset or a software reset.

Register 0x05A: DCRU Reset

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	Reserved	X
Bit 3	R/W	Reserved	X
Bit 2	R/W	Reserved	X
Bit 1	R/W	Reserved	X
Bit 0	R/W	Reserved	X

Writing to this register performs a software reset of the DCRU. The software reset will disrupt the serial receive interface. Any FIFOs associated with the recovered clock (JAT) must be reset after the DCRU is reset.

Register 0x05C: CRSI Configuration

Bit	Type	Function	Default
Bit 7	R/W	SDINV	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	SENB	0
Bit 4	R/W	Reserved	0
Bit 3		Unused	X
Bit 2	R	LOTI	X
Bit 1	R	ROOLI	X
Bit 0	R	DOOLI	X

DOOLI:

The DOOLI bit is the data out of lock interrupt status bit. DOOLI is set high when the DOOLV bit changes state, indicating that either the CRU has locked to the incoming data stream or has gone out of lock. DOOLI is cleared when this register is read.

ROOLI:

The ROOLI bit is the reference out of lock interrupt status bit. ROOLI is set high when the ROOLV register changes state, indicating that either the PLL is locked to the reference clock REFCLK or is in out of lock. ROOLI is cleared when this register is read.

LOTI:

The LOTI bit is the loss of transition interrupt status bit. LOTI is set high when a loss of transition event occurs. A loss of transition is defined as either the SD input set low or more than 96 consecutive ones or zeros received. LOTI is cleared when this register is read.

SENB:

The loss of signal transition detector enable (SENB) bit enables the declaration of loss of transition (LOT) when more than 96 consecutive ones or zeros occurs in the receive data. When SENB is a logic zero, a loss of transition is declared when more than 96 consecutive ones or zeros occurs in the receive data or when the SD input is low. When SENB is a logic one, a loss of transition is declared only when the SD input is low.

SDINV:

The signal detect input invert (SDINV) controls the polarity of the SD input. The value of the SD input is logically XOR'ed with the value of the SDINV register. Therefore, when SDINV is a logic zero, valid signal power is indicated by the SD input high. When SDINV is a logic one, valid signal power is indicated by the SD input low.

Register 0x05D: CRSI Status

Bit	Type	Function	Default
Bit 7	R	LOCK	X
Bit 6	R	LOTV	X
Bit 5	R	ROOLV	X
Bit 4	R	DOOLV	X
Bit 3		Unused	X
Bit 2	R/W	LOTE	0
Bit 1	R/W	ROOLE	0
Bit 0	R/W	DOOLE	0

DOOLE:

The DOOLE bit is an interrupt enable for the recovered data out of lock status. When DOOLE is set to logic one, an interrupt is generated upon assertion and negation events of the DOOLV register. When ROOLE is set low, changes in the DOOL status do not generate an interrupt.

ROOLE:

The ROOLE bit enables the reference out of lock indication interrupt. When ROOLE is set high, an interrupt is generated upon assertion and negation events of the ROOLV register. When ROOLE is set low, changes in the ROOL status do not generate an interrupt.

LOTE:

The LOTE bit enables the loss of transition indication interrupt. When LOTE is set high, an interrupt is generated upon assertion events of the LOTV register. When LOTE is set low, changes in the LOTV status do not generate an interrupt.

DOOLV:

The recovered data out of lock status indicates the clock recovery phase locked loop is unable to recover and lock to the input data stream. DOOLV is a logic one if the divided down recovered clock frequency is not within approximately 488ppm of the REFCLK frequency or if no transitions have occurred on the RXD input for more than 96 bits.

ROOLV:

The recovered reference out of lock status indicates the clock recovery phase locked loop is unable to lock to the reference clock on REFCLK. ROOLV is a logic one if the divided down synthesized clock frequency is not within approximately 488ppm of the REFCLK frequency. At startup, ROOLV may remain high for several hundred millisecond while the PLL obtains lock.

LOTV:

The loss of transition status indicates the receive power is lost or at least 97 consecutive ones or zeros have been received. LOTV is a logic zero if the SD input is high or less than 97 consecutive ones or zeros have been received. LOTV is a logic one if the SD input is low or more than 96 consecutive ones or zeros have been received.

LOCK:

The CRU reference locking status indicates if the CRU is locking to the reference clock or locking to the receive data. LOCK is a logic zero if the CRU is locking or locked to the reference clock. LOCK is a logic one if the CRU is locking or locked to the receive data. LOCK is invalid if the CRU is not used.

Register 0x060: RXCP Configuration 1

Bit	Type	Function	Default
Bit 7	R/W	DDSCR	0
Bit 6	R/W	HDSCR	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	HCSADD	1
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

HCSADD:

The HCSADD bit controls the addition of the coset polynomial, $x^6+x^4+x^2+1$, to the HCS octet prior to comparison. When HCSADD is a logic one, the polynomial is added, and the resulting HCS is compared. When HCSADD is a logic zero, the polynomial is not added, and the unmodified HCS is compared.

HDSCR:

HDSCR enables the self-synchronous $x^{43} + 1$ descrambler to continue running through the bytes which should contain the ATM cell headers. When HSCR is set low, the descrambling polynomial will function only over the ATM payload bytes. When HDSCR is set high, the descrambling polynomial will function over all bytes, including the 5 ATM header bytes. This function is available for use with PPP packets and flags which are scrambled at the source to prevent the generation of "killer" sequences.

DDSCR:

The DDSCR bit controls the descrambling of the cell payload with the polynomial $x^{43} + 1$. When DDSCR is set high, cell payload descrambling is disabled. When DDSCR is set low, payload descrambling is enabled.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x061: RXCP Configuration 2

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	IDLEPASS	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

IDLEPASS:

The IDLEPASS bit controls the function of the Idle Cell filter. When IDLEPASS is written with a logic zero, all cells that match the Idle Cell Header Pattern and Idle Cell Header Mask are filtered out. When IDLEPASS is a logic one, the Idle Cell Header Pattern and Mask registers are ignored. The default state of this bit and the bits in the Idle Cell Header Mask and Idle Cell Header Pattern Registers enable the dropping of idle cells.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x062: RXCP FIFO/UTOPIA Control and Configuration

Bit	Type	Function	Default
Bit 7	R/W	RXPTYP	0
Bit 6		Unused	X
Bit 5	R/W	RCAINV	0
Bit 4	R/W	RCALEVEL0	1
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	FIFORST	0

FIFORST:

The FIFORST bit is used to reset the channel four-cell receive buffer. When FIFORST is set low, the channel buffer operates normally. When FIFORST is set high, the buffer is immediately emptied and ignores writes. The buffer remains empty and continues to ignore writes until a logic zero is written to FIFORST.

FIFORST must be set high before the per-channel FIFO reset in the RFCLK DLL is asserted. FIFORST must be set low after the per-channel FIFO reset in the RFCLK DLL is asserted.

RCALEVEL0:

The RCA level 0 bit, RCALEVEL0, determines when the RCA transitions low for Level 2 operation. When RCALEVEL0 is set high, a high-to-low transition on output RCA indicates that the receive FIFO is empty and RCA will de-assert on the rising RFCLK edge after word 27 (of the 27 word cell structure) is output. When RCALEVEL0 is set low, a high-to-low transition on output RCA indicates that the receive FIFO is near empty and RCA will de-assert on the rising RFCLK edge after word 23 (of the 27 word cell structure) is output.

RCAINV:

The RCAINV bit inverts the polarity of the RCA output signal for Level 2 operation. When RCAINV is a logic one, the polarity of RCA is inverted (RCA at logic zero means there is a receive cell available to be read). When RCAINV is a logic zero, the polarity of RCA is not inverted.

RXPTYP:

The RXPTYP bit selects even or odd parity for output RPRTY for Level 2 operation. When set high, output RPRTY is the even parity bit for outputs RDAT[15:0]. When RXPTYP is set low, RPRTY is the odd parity bit for outputs RDAT[15:0].

Register 0x063: RXCP Interrupt Enable and Count Status

Bit	Type	Function	Default
Bit 7	R	XFERI	X
Bit 6	R	OVR	X
Bit 5		Unused	X
Bit 4	R/W	XFERE	0
Bit 3	R/W	OOCDE	0
Bit 2	R/W	HCSE	0
Bit 1	R/W	FOVRE	0
Bit 0	R/W	LCDE	0

LCDE:

The LCDE bit enables the generation of an interrupt due to a change in the LCD state. When LCDE is set high, the interrupt is enabled.

FOVRE:

The FOVRE bit enables the generation of an interrupt due to a FIFO overrun error condition. When FOVRE is set high, the interrupt is enabled.

HCSE:

The HCSE bit enables the generation of an interrupt due to the detection of a corrected or an uncorrected HCS error. When HCSE is set high, the interrupt is enabled.

OOCDE:

The OOCDE bit enables the generation of an interrupt due to a change in cell delineation state. When OOCDE is set high, the interrupt is enabled.

XFERE:

The XFERE bit enables the generation of an interrupt when an accumulation interval is completed and new values are stored in the RXCP Count registers. When XFERE is set high, the interrupt is enabled.

OVR:

The OVR bit is the overrun status of the RXCP Performance Monitoring Count registers. A logic one in this bit position indicates that a previous transfer (indicated by XFERI being logic one) has not been acknowledged before the next accumulation interval has occurred and that the contents of the RXCP Count registers have been overwritten. OVR is set low when this register is read.

XFERI:

The XFERI bit indicates that a transfer of RXCP Performance Monitoring Count data has occurred. A logic one in this bit position indicates that the RXCP Count registers have been updated. This update is initiated by writing to one of the RXCP Count register locations, to the S/UNI-1x155 Master Reset and Identity register or the channel Master Interrupt Status register. XFERI is set low when this register is read.

Register 0x064: RXCP Status/Interrupt Status

Bit	Type	Function	Default
Bit 7	R	OOCDV	X
Bit 6	R	LCDV	X
Bit 5		Unused	X
Bit 4	R	OOCDI	X
Bit 3		Unused	X
Bit 2	R	HCSI	X
Bit 1	R	FOVRI	X
Bit 0	R	LCDI	X

LCDI:

The LCDI bit is set high when there is a change in the loss of cell delineation (LCD) state. This bit is reset immediately after a read to this register.

FOVRI:

The FOVRI bit is set high when an attempt is made to write into the channel buffer when it is already full. This bit is reset immediately after a read to this register. Continuous over-writing of the channel buffer results in only one interrupt.

HCSI:

The UHCSI bit is set high when an HCS error is detected. This bit is reset immediately after a read to this register.

OOCDI:

The OOCDI bit is set high when the RXCP enters or exits the SYNC state. The OOCDV bit indicates whether the RXCP is in the SYNC state or not. The OOCDI bit is reset immediately after a read to this register.

LCDV:

The LCDV bit gives the Loss of Cell Delineation state. When LCD is high, an out of cell delineation (OCD) defect has persisted for the number of cells specified in the LCD Count Threshold register. When LCD is low, no OCD has persisted for the number of cells specified in the LCD Count Threshold register. The cell time period can be varied by using the LCDC[7:0] register bits in the RXCP LCD Count Threshold register.

OOCDV:

The OOCDV bit indicates the cell delineation state. When OOCDV is high, the cell delineation state machine is in the 'HUNT' or 'PRESYNC' state and is hunting for the cell boundaries. When OOCDV is low, the cell delineation state machine is in the 'SYNC' state and cells are passed through the receive FIFO.

Register 0x065: RXCP LCD Count Threshold MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	LCDC[10]	0
Bit 1	R/W	LCDC[9]	0
Bit 0	R/W	LCDC[8]	1

Register 0x066: RXCP LCD Count Threshold LSB

Bit	Type	Function	Default
Bit 7	R/W	LCDC[7]	0
Bit 6	R/W	LCDC[6]	1
Bit 5	R/W	LCDC[5]	1
Bit 4	R/W	LCDC[4]	0
Bit 3	R/W	LCDC[3]	1
Bit 2	R/W	LCDC[2]	0
Bit 1	R/W	LCDC[1]	0
Bit 0	R/W	LCDC[0]	0

LCDC[10:0]:

The LCDC[10:0] bits represent the number of consecutive cell periods the receive cell processor must be out of cell delineation before loss of cell delineation (LCD) is declared. Likewise, LCD is not de-asserted until receive cell processor is in cell delineation for the number of cell periods specified by LCDC[10:0].

The default value of LCD[10:0] is 360, which translates to an average cell period of 0.71 µs and a default LCD integration period of 255 µs.

Register 0x067: RXCP Idle Cell Header Pattern

Bit	Type	Function	Default
Bit 7	R/W	GFC[3]	0
Bit 6	R/W	GFC[2]	0
Bit 5	R/W	GFC[1]	0
Bit 4	R/W	GFC[0]	0
Bit 3	R/W	PTI[2]	0
Bit 2	R/W	PTI[1]	0
Bit 1	R/W	PTI[0]	0
Bit 0	R/W	CLP	1

CLP:

The CLP bit contains the pattern to match in the eighth bit of the fourth octet of the 53-octet cell, in conjunction with the Match Header Mask Register. The IDLEPASS bit in the RXCP Configuration 2 Register must be set to logic zero to enable dropping of cells matching this pattern.

PTI[2:0]:

The PTI[2:0] bits contain the pattern to match in the fifth, sixth, and seventh bits of the fourth octet of the 53-octet cell, in conjunction with the Idle Cell Header Mask Register. The IDLEPASS bit in the RXCP Configuration 2 Register must be set to logic zero to enable dropping of cells matching this pattern.

GFC[3:0]:

The GFC[3:0] bits contain the pattern to match in the first, second, third, and fourth bits of the first octet of the 53-octet cell, in conjunction with the Idle Cell Header Mask Register. The IDLEPASS bit in the RXCP Configuration 2 Register must be set to logic zero to enable dropping of cells matching this pattern. Note that an all-zeros pattern must be present in the VPI and VCI fields of the idle or unassigned cell.

Register 0x068: RXCP Idle Cell Header Mask

Bit	Type	Function	Default
Bit 7	R/W	MGFC[3]	1
Bit 6	R/W	MGFC[2]	1
Bit 5	R/W	MGFC[1]	1
Bit 4	R/W	MGFC[0]	1
Bit 3	R/W	MPTI[2]	1
Bit 2	R/W	MPTI[1]	1
Bit 1	R/W	MPTI[0]	1
Bit 0	R/W	MCLP	1

MCLP:

The CLP bit contains the mask pattern for the eighth bit of the fourth octet of the 53-octet cell. This mask is applied to the Idle Cell Header Pattern Register to select the bits included in the cell filter. A logic one in this bit position enables the MCLP bit in the pattern register to be compared. A logic zero causes the masking of the MCLP bit.

MPTI[2:0]:

The MPTI[2:0] bits contain the mask pattern for the fifth, sixth, and seventh bits of the fourth octet of the 53-octet cell. This mask is applied to the Idle Cell Header Pattern Register to select the bits included in the cell filter. A logic one in any bit position enables the corresponding bit in the pattern register to be compared. A logic zero causes the masking of the corresponding bit.

MGFC[3:0]:

The MGFC[3:0] bits contain the mask pattern for the first, second, third, and fourth bits of the first octet of the 53-octet cell. This mask is applied to the Idle Cell Header Pattern Register to select the bits included in the cell filter. A logic one in any bit position enables the corresponding bit in the pattern register to be compared. A logic zero causes the masking of the corresponding bit.

Register 0x06A: RXCP HCS Error Count

Bit	Type	Function	Default
Bit 7	R	HCS[7]	X
Bit 6	R	HCS[6]	X
Bit 5	R	HCS[5]	X
Bit 4	R	HCS[4]	X
Bit 3	R	HCS[3]	X
Bit 2	R	HCS[2]	X
Bit 1	R	HCS[1]	X
Bit 0	R	HCS[0]	X

HCS[7:0]:

The HCS[7:0] bits indicate the number of HCS error events that occurred during the last accumulation interval. The contents of these registers are valid a maximum of 40 RCLK periods after a transfer is triggered by a write to one of RXCP's performance monitor.

The count can also be polled by writing to the S/UNI-1x155 Master Reset and Identity register (0x000). Writing to register address 0x000 loads all counter registers in the channel and APS link.

The count can also be polled by writing to the channel Master Interrupt Status register (0x007). Writing to register 0x007 loads all counter registers in the RSOP, RLOP, RPOP, SPTB, SSTB, RXCP, TXCP, RXFP, and TXFP blocks of the channel.

Register 0x06B: RXCP Receive Cell Count LSB

Bit	Type	Function	Default
Bit 7	R	RCELL[7]	X
Bit 6	R	RCELL[6]	X
Bit 5	R	RCELL[5]	X
Bit 4	R	RCELL[4]	X
Bit 3	R	RCELL[3]	X
Bit 2	R	RCELL[2]	X
Bit 1	R	RCELL[1]	X
Bit 0	R	RCELL[0]	X

Register 0x06C: RXCP Receive Cell Count

Bit	Type	Function	Default
Bit 7	R	RCELL[15]	X
Bit 6	R	RCELL[14]	X
Bit 5	R	RCELL[13]	X
Bit 4	R	RCELL[12]	X
Bit 3	R	RCELL[11]	X
Bit 2	R	RCELL[10]	X
Bit 1	R	RCELL[9]	X
Bit 0	R	RCELL[8]	X

Register 0x06D: RXCP Receive Cell Count MSB

Bit	Type	Function	Default
Bit 7	R	RCELL[23]	X
Bit 6	R	RCELL[22]	X
Bit 5	R	RCELL[21]	X
Bit 4	R	RCELL[20]	X
Bit 3	R	RCELL[19]	X
Bit 2	R	RCELL[18]	X
Bit 1	R	RCELL[17]	X
Bit 0	R	RCELL[16]	X

RCELL[23:0]:

The RCELL[23:0] bits indicate the number of cells received and written into the receive FIFO during the last accumulation interval. Cells received and filtered due to HCS errors or Idle cell matches are not counted. The counter should be polled every second to avoid saturation. The contents of these registers are valid a maximum of 67 RCLK periods after a transfer is triggered by a write to one of RXCP's performance monitor counters.

The count can also be polled by writing to the S/UNI-1x155 Master Reset and Identity register (0x000). Writing to register address 0x000 loads all counter registers in the channel and APS link.

The count can also be polled by writing to the channel Master Interrupt Status register (0x007). Writing to register 0x007 loads all counter registers in the RSOP, RLOP, RPOP, SPTB, SSTB, RXCP, TXCP, RXFP, and TXFP blocks of the channel.

Register 0x06E: RXCP Idle Cell Counter LSB

Bit	Type	Function	Default
Bit 7	R	ICELL[7]	X
Bit 6	R	ICELL[6]	X
Bit 5	R	ICELL[5]	X
Bit 4	R	ICELL[4]	X
Bit 3	R	ICELL[3]	X
Bit 2	R	ICELL[2]	X
Bit 1	R	ICELL[1]	X
Bit 0	R	ICELL[0]	X

Register 0x06F: RXCP Idle Cell Counter

Bit	Type	Function	Default
Bit 7	R	ICELL[15]	X
Bit 6	R	ICELL[14]	X
Bit 5	R	ICELL[13]	X
Bit 4	R	ICELL[12]	X
Bit 3	R	ICELL[11]	X
Bit 2	R	ICELL[10]	X
Bit 1	R	ICELL[9]	X
Bit 0	R	ICELL[8]	X

Register 0x070: RXCP Idle Cell Count MSB

Bit	Type	Function	Default
Bit 7	R	ICELL[23]	X
Bit 6	R	ICELL[22]	X
Bit 5	R	ICELL[21]	X
Bit 4	R	ICELL[20]	X
Bit 3	R	ICELL[19]	X
Bit 2	R	ICELL[18]	X
Bit 1	R	ICELL[17]	X
Bit 0	R	ICELL[16]	X

ICELL[23:0]:

The ICELL[23:0] bits indicate the number of idle cells received during the last accumulation interval. The counter should be polled every second to avoid saturation. The contents of these registers are valid a maximum of 67 RCLK periods after a transfer is triggered by a write to one of RXCP's performance monitor counters.

The count can also be polled by writing to the S/UNI-1x155 Master Reset and Identity register (0x000). Writing to register address 0x000 loads all counter registers in the channel and APS link.

The count can also be polled by writing to the channel Master Interrupt Status register (0x007). Writing to register 0x007 loads all counter registers in the RSOP, RLOP, RPOP, SPTB, SSTB, RXCP, TXCP, RXFP, and TXFP blocks of the channel.

Register 0x080: TXCP Configuration 1

Bit	Type	Function	Default
Bit 7	R/W	TPTYP	0
Bit 6	R/W	TCALEVEL0	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	HCSB	0
Bit 2	R/W	HCSADD	1
Bit 1	R/W	DSCR	0
Bit 0	R/W	FIFORST	0

FIFORST:

The FIFORST bit is used to reset the channel four cell transmit buffer. When FIFORST is set to logic zero, the buffer operates normally. When FIFORST is set to logic one, the buffer is immediately emptied and ignores writes. The buffer remains empty and continues to ignore writes until a logic zero is written to FIFORST. Null/unassigned cells are transmitted until a subsequent cell is written to the buffer.

The FIFORST must be set high before the per-channel reset in the TFCLK DLL is asserted. The FIFORST must be set low after the per-channel reset in the TFCLK DLL is deasserted.

DSCR:

The DSCR bit controls the scrambling of the cell payload. When DSCR is a logic one, cell payload scrambling is disabled. When DSCR is a logic zero, payload scrambling is enabled.

HCSADD:

The HCSADD bit controls the addition of the coset polynomial, $x^6+x^4+x^2+1$, to the HCS octet prior to insertion in the synchronous payload envelope. When HCSADD is a logic one, the polynomial is added, and the resulting HCS is inserted. When HCSADD is a logic zero, the polynomial is not added, and the unmodified HCS is inserted. HCSADD takes effect unconditionally regardless of whether a null/unassigned cell is being transmitted or whether the HCS octet has been read from the FIFO.

HCSB:

The active low HCSB bit enables the internal generation and insertion of the HCS octet into the transmit cell stream. When HCSB is logic zero, the HCS is generated and inserted internally.

TCALEVEL0:

The TCA level control (TCALEVEL0) determines when the TCA will transition low as the FIFO fills for Level 2 operation. When TCALEVEL0 is logic zero, TCA will de-assert on the same rising TFCLK edge that samples word 21 of the 27 word ATM cell structure. When TCALEVEL0 is logic one, TCA will de-assert on the same rising TFCLK edge that samples word 26 of the 27 word ATM cell structure.

TPTYP:

The TPTYP bit selects even or odd parity for input TPRTY for Level 2 operation. When set to logic one, input TPRTY is the even parity bit for the TDAT input bus. When set to logic zero, input TPRTY is the odd parity bit for the TDAT input bus.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x081: TXCP Configuration 2

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	TCAINV	0
Bit 3	R/W	FIFODP[1]	0
Bit 2	R/W	FIFODP[0]	0
Bit 1	R/W	DHCS	0
Bit 0	R/W	HCSCTLEB	0

HCSCTLEB:

The active low HCS control enable, HCSCTLEB bit enables the XORing of the HCS Control byte with the generated HCS. When set to logic zero, the HCS Control byte provided in the third word of the 27 word data structure is XORed with the generated HCS. When set to logic one, XORing is disabled and the HCS Control byte is ignored.

For normal operation, the HCS Control byte in the ATM cell structure transferred on the system interface should always be 0x00. If not, the HCSCTLEB register should be set to logic one to prevent corruption of the HCS byte.

DHCS:

The DHCS bit controls the insertion of HCS errors for diagnostic purposes. When DHCS is set to logic one, the HCS octet is inverted prior to insertion in the synchronous payload envelope. DHCS takes effect unconditionally regardless of whether a null/unassigned cell is being transmitted or whether the HCS octet has been read from the FIFO. DHCS occurs after any error insertion caused by the Control Byte in the 27-word data structure.

FIFODP[1:0]:

The FIFODP[1:0] bits determine the transmit FIFO cell depth at which TCA is de-asserted. FIFO depth control may be important in systems where the cell latency through the TXCP must be minimized. When the FIFO is filled to the specified depth, the transmit cell available signal, TCA is deasserted. Note that regardless of what fill level FIFODP[1:0] is set to, the transmit cell processor can store 4 complete cells. The selectable FIFO cell depths are shown below:

FIFODP[1]	FIFODP[0]	FIFO DEPTH
0	0	4 cells
0	1	3 cells
1	0	2 cells
1	1	1 cell

TCAINV:

The TCAINV bit inverts the polarity of the TCA output signal for Level 2 operation. When TCAINV is a logic one, the polarity of TCA is inverted (TCA at logic zero means there is transmit cell space available to be written to). When TCAINV is a logic zero, the polarity of TCA is not inverted.

Register 0x082: TXCP Transmit Cell Count Status

Bit	Type	Function	Default
Bit 7	R/W	XFERE	0
Bit 6	R	XFERI	X
Bit 5	R	OVR	X
Bit 4		Unused	X
Bit 3	R/W	Reserved	1
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

OVR:

The OVR bit is the overrun status of the Transmit Cell Count registers. A logic one in this bit position indicates that a previous transfer (indicated by XFERI being logic one) has not been acknowledged before the next accumulation interval has occurred and that the contents of the Transmit Cell Count registers have been overwritten. OVR is set low when this register is read.

XFERI:

The XFERI bit indicates that a transfer of Transmit Cell Count data has occurred. A logic one in this bit position indicates that the Transmit Cell Count registers have been updated. This update is initiated by writing to one of the Transmit Cell Count register locations, to the S/UNI-1x155 Master Reset and Identity register or to the channel Master Interrupt Status register. XFERI is set low when this register is read.

XFERE:

The XFERE bit enables the generation of an interrupt when an accumulation interval is completed and new values are stored in the Transmit Cell Count registers. When XFERE is set high, the interrupt is enabled.

Reserved:

These bits should be set to their default values for proper operation.

Register 0x083: TXCP Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7	R/W	TPRTYE	0
Bit 6	R/W	FOVRE	0
Bit 5	R/W	TSOCE	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	TPRTYI	X
Bit 1	R	FOVRI	X
Bit 0	R	TSOCI	X

TSOCI:

The TSOCI bit is set high when the TSOC input is sampled high during any position other than the first word of the selected data structure. The write address counter is reset to the first word of the data structure when TSOC is sampled high. This bit is reset immediately after a read to this register.

FOVRI:

The FOVRI bit is set high when an attempt is made to write into the FIFO when it is already full. This bit is reset immediately after a read to this register.

TPRTYI:

The TPRTYI bit indicates if a parity error was detected on the TDAT input bus. When logic one, the TPRTYI bit indicates a parity error over the active TDAT bus. This bit is cleared when this register is read. Odd or even parity is selected using the TPTYP bit.

TSOCE:

The TSOCE bit enables the generation of an interrupt when the TSOC input is sampled high during any position other than the first word of the selected data structure. When TSOCE is set to logic one, the interrupt is enabled.

FOVRE:

The FOVRE bit enables the generation of an interrupt due to an attempt to write the FIFO when it is already full. When FOVRE is set to logic one, the interrupt is enabled.

TPRTYE:

The TPRTYE bit enables transmit parity interrupts. When set to logic one, parity errors are indicated on INTB and TPRTYI. When set to logic zero, parity errors are indicated using bit TPRTYI, but are not indicated on output INTB.

Register 0x084: TXCP Idle Cell Header Control

Bit	Type	Function	Default
Bit 7	R/W	GFC[3]	0
Bit 6	R/W	GFC[2]	0
Bit 5	R/W	GFC[1]	0
Bit 4	R/W	GFC[0]	0
Bit 3	R/W	PTI[2]	0
Bit 2	R/W	PTI[1]	0
Bit 1	R/W	PTI[0]	0
Bit 0	R/W	CLP	1

CLP:

The CLP bit contains the eighth bit position of the fourth octet of the idle/unassigned cell pattern. Cell rate decoupling is accomplished by transmitting idle cells when the TXCP detects that no outstanding cells exist in the transmit FIFO.

PTI[2:0]:

The PTI[2:0] bits contain the fifth, sixth, and seventh bit positions of the fourth octet of the idle/unassigned cell pattern. Idle cells are transmitted when the TXCP detects that no outstanding cells exist in the transmit FIFO.

GFC[3:0]:

The GFC[3:0] bits contain the first, second, third, and fourth bit positions of the first octet of the idle/unassigned cell pattern. Idle/unassigned cells are transmitted when the TXCP detects that no outstanding cells exist in the transmit FIFO. The all zeros pattern is transmitted in the VCI and VPI fields of the idle cell.

Register 0x085: TXCP Idle Cell Payload Control

Bit	Type	Function	Default
Bit 7	R/W	PAYLD[7]	0
Bit 6	R/W	PAYLD[6]	1
Bit 5	R/W	PAYLD[5]	1
Bit 4	R/W	PAYLD[4]	0
Bit 3	R/W	PAYLD[3]	1
Bit 2	R/W	PAYLD[2]	0
Bit 1	R/W	PAYLD[1]	1
Bit 0	R/W	PAYLD[0]	0

PAYLD[7:0]:

The PAYLD[7:0] bits contain the pattern inserted in the idle cell payload. Idle cells are insertedwhen the TXCP detects that the transmit FIFO contains no outstanding cells. PAYLD[7] is the most significant bit and is the first bit transmitted. PAYLD[0] is the least significant bit.

Register 0x086: TXCP Transmit Cell Count LSB

Bit	Type	Function	Default
Bit 7	R	TCELL[7]	X
Bit 6	R	TCELL[6]	X
Bit 5	R	TCELL[5]	X
Bit 4	R	TCELL[4]	X
Bit 3	R	TCELL[3]	X
Bit 2	R	TCELL[2]	X
Bit 1	R	TCELL[1]	X
Bit 0	R	TCELL[0]	X

Register 0x087: TXCP Transmit Cell Count

Bit	Type	Function	Default
Bit 7	R	TCELL[15]	X
Bit 6	R	TCELL[14]	X
Bit 5	R	TCELL[13]	X
Bit 4	R	TCELL[12]	X
Bit 3	R	TCELL[11]	X
Bit 2	R	TCELL[10]	X
Bit 1	R	TCELL[9]	X
Bit 0	R	TCELL[8]	X

Register 0x088: TXCP Transmit Cell Count MSB

Bit	Type	Function	Default
Bit 7	R	TCELL[23]	X
Bit 6	R	TCELL[22]	X
Bit 5	R	TCELL[21]	X
Bit 4	R	TCELL[20]	X
Bit 3	R	TCELL[19]	X
Bit 2	R	TCELL[18]	X
Bit 1	R	TCELL[17]	X
Bit 0	R	TCELL[16]	X

TCELL[23:0]:

The TCELL[23:0] bits indicate the number of cells read from the transmit FIFO and inserted into the transmission stream during the last accumulation interval. Idle cells inserted into the transmission stream are not counted. A write to any one of the TXCP Transmit Cell Counter registers loads the registers with the current counter value and resets the internal count to zero.

The count can also be polled by writing to the S/UNI-1x155 Master Reset and Identity register (0x000). Writing to register address 0x000 loads all counter registers in the channel and APS link.

The count can also be polled by writing to the channel Master Interrupt Status register (0x007). Writing to register 0x007 loads all counter registers in the RSOP, RLOP, RPOP, SPTB, SSTB, RXCP, TXCP, RXFP, and TXFP blocks of the channel.

Register 0x094: Receive Cell/Packet Counter LSB

Bit	Type	Function	Default
Bit 7	R	RCNT[7]	X
Bit 6	R	RCNT[6]	X
Bit 5	R	RCNT[5]	X
Bit 4	R	RCNT[4]	X
Bit 3	R	RCNT[3]	X
Bit 2	R	RCNT[2]	X
Bit 1	R	RCNT[1]	X
Bit 0	R	RCNT[0]	X

Register 0x095: Receive Cell/Packet Counter

Bit	Type	Function	Default
Bit 7	R	RCNT[15]	X
Bit 6	R	RCNT[14]	X
Bit 5	R	RCNT[13]	X
Bit 4	R	RCNT[12]	X
Bit 3	R	RCNT[11]	X
Bit 2	R	RCNT[10]	X
Bit 1	R	RCNT[9]	X
Bit 0	R	RCNT[8]	X

Register 0x096: Receive Cell/Packet Counter MSB

Bit	Type	Function	Default
Bit 7	R	RCNT[23]	X
Bit 6	R	RCNT[22]	X
Bit 5	R	RCNT[21]	X
Bit 4	R	RCNT[20]	X
Bit 3	R	RCNT[19]	X
Bit 2	R	RCNT[18]	X
Bit 1	R	RCNT[17]	X
Bit 0	R	RCNT[16]	X

RCNT[23:0]:

The RCNT[23:0] bits indicate the number of cells or packets received during the last accumulation interval. When the channel is configured for ATM traffic, the number of valid received ATM cells are counted. When the channel is configured for packet trace, the number of end of packets are counted.

This counter exists after the RXCP/RXFP FIFO allowing it to count the number of actual received items. However, when compared to the performance counters in RXCP/RXFP, RCNT[23:0] may differ slightly due to the number of items stored in the RXCP/RXFP FIFO.

The count is polled by writing to the S/UNI-1x155 Master Reset and Identity register (0x000). Writing to register address 0x000 loads all counter registers in all channels and APS links.

The count can also be polled by writing to the channel Master Interrupt Status register (offset 0x07). Writing to register offset 0x07 loads all counter registers in the RSOP, RLOP, RPOP, SPTB, SSTB, RXCP, TXCP, RXFP, and TXFP blocks of the channel.

Register 0x098: JAT Configuration #1

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	FERRI	X
Bit 3	R	RUN	X
Bit 2	R	ERROR	X
Bit 1	R	ERRORI	X
Bit 0	R/W	ERRORE	0

ERRORE:

The JAT error interrupt enable controls the assertion of the INTB output when ERROR is high. When ERRORE is set high, an interrupt is generated upon assertion event of the ERROR register. When ERRORE is set low, changes in the ERROR status do not generate an interrupt.

ERRORI:

The error event register bit ERRORI indicates the ERROR register bit has been a logic one. When the ERROR register changes from a logic zero to a logic one, the ERRORI register bit is set to logic one. The ERRORI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

ERROR:

The delay line error register ERROR indicates the JAT is currently at the end of the delay line. ERROR is set high when the JAT tries to move beyond either end of the delay line.

RUN:

The JAT lock status register bit RUN indicates the JAT has found an initial delay line lock . When the JAT is attempting to recover the incoming serial stream, RUN is set high. The RUN register bit is cleared only by a system reset or a software reset.

FERRI:

The line loopback FIFO error status (FERRI) indicates that the 8-byte line loopback FIFO has overrun or underrun. The FERRI bit is set high when the loopback FIFO corrupts the transmit data stream due to a FIFO overrun or underrun. The FERRI bit clears when the register is read, thus acknowledging the error has occurred.

Register 0x099: JAT Configuration #2

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	FRST	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	FORCE55	0

FORCE55:

The diagnostic serial transmit enable (FORCE55) forces the outgoing serial transmit stream to alternating ones and zeros. When FORCE55 is set high, the serial transmit stream is a 77.76MHz clock. When FORCE55 is set low, the serial interface operates normally.

FRST:

The line loopback FIFO reset control allows the line loopback path to be initialized. When FRST is high, the bit FIFO in the line loopback path in the JAT is held in reset. When FRST is low, the FIFO operates normally.

The FRST control should be toggled when the receive interface experiences severe errors such as loss of frame (LOF) or loss of signal (LOS) during SLLE operation.

Reserved:

The reserved bit must be programmed to logic zero for proper operation.

Register 0x0A0: RXFP Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	FCSPASS	0
Bit 5	R/W	RPAINV	0
Bit 4	R/W	FCSSEL[1]	1
Bit 3	R/W	FCSSEL[0]	0
Bit 2	R/W	RXPTYP	0
Bit 1	R/W	DDSCR	1
Bit 0	R/W	FIFORST	0

FIFORST:

The FIFORST bit is used to reset the channel 256-byte receive buffer. When FIFORST is set low, the channel buffer operates normally. When FIFORST is set high, the buffer is immediately emptied and ignores writes. The buffer remains empty and continues to ignore writes until a logic zero is written to FIFORST.

The FIFORST must be set high before the per-channel FIFO reset in the RFCLK DLL is asserted. The FIFORST must be set low after the per-channel FIFO reset in the RFCLK DLL is deasserted.

DDSCR:

The DDSCR bit controls the descrambling of the frame payload with the polynomial $x^{43} + 1$. When DDSCR is set low, frame payload descrambling is disabled. When DDSCR is set high, payload descrambling is enabled.

RXPTYP:

The RXPTYP bit selects even or odd parity for output RPRTY for Level 2 operation. When set high, output RPRTY is the even parity bit for outputs RDAT[15:0]. When RXPTYP is set low, RPRTY is the odd parity bit for outputs RDAT[15:0].

FCSSEL[1:0]:

The Frame Control Sequence select (FCSSEL[1:0]) bits control the FCS calculation according to the table below. The FCS is calculated over the whole packet data, after byte destuffing and descrambling.

FCSSEL[1:0]	FCS Operation
00	No FCS calculated
01	CRC-16.ISO-3309 (2 bytes)

10	CRC-32 (4 bytes)
11	Reserved

RPAINV:

The RPAINV bit inverts the polarity of the RPA output signal for Level 2 operation. When RPAINV is a logic one, the polarity of RPA is inverted (RPA at logic zero means there is a receive cell available to be read). When RPAINV is a logic zero, the polarity of RPA is not inverted.

FCSPASS:

FCSPASS determines if the FCS field will be passed through the system interface or stripped. When FCSPASS is set to logic one, the POS frame FCS field is written into the FIFO as part of the packet, and can thus be read through the system interface. When FCSPASS is set to logic zero, the FCS field is stripped from the POS frame.

Reserved:

The reserved bit must be programmed to logic zero for proper operation.

Register 0x0A1: RXFP Configuration/Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	MINLE	0
Bit 4	R/W	MAXLE	0
Bit 3	R/W	ABRTE	0
Bit 2	R/W	FCSE	0
Bit 1	R/W	FOVRE	0
Bit 0	R/W	Reserved	0

FOVRE:

The FOVRE bit enables the generation of an interrupt due to a channel buffer overrun error condition. When FOVRE is set high, the interrupt is enabled.

FCSE:

The FCSE bit enables the generation of an interrupt due to the detection of an FCS error. When FCSE is set high, the interrupt is enabled.

ABRTE:

The Abort Packet Enable bit enables the generation of an interrupt due to the reception of an aborted packet. When ABRTE is set high, the interrupt is enabled.

MAXLE:

The Maximum Length Packet Enable bit enables the generation of an interrupt due to the reception of a packet exceeding the programmable maximum packet length. When MAXLE is set high, the interrupt is enabled.

MINLE:

The Minimum Length Packet Enable bit enables the generation of an interrupt due to the reception of a packet that is smaller than the programmable minimum packet length. When MINLE is set high, the interrupt is enabled.

Reserved:

The reserved bit must be programmed to logic zero for proper operation.

Register 0x0A2: RXFP Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	MINLI	X
Bit 4	R	MAXLI	X
Bit 3	R	ABRTI	X
Bit 2	R	FCSI	X
Bit 1	R	FOVRI	X
Bit 0		Unused	X

FOVRI:

The FOVRI bit indicates an interrupt due to a channel buffer overrun error condition. This interrupt can be masked using FOVRE.

FCSI:

The FCSI bit indicates an interrupt due to the detection of an FCS error. This interrupt can be masked using FCSE.

ABRTI:

The ABRTI bit indicates the generation of an interrupt due to the reception of an aborted packet. This interrupt can be masked using ABRTE.

MAXLI:

The MAXLI bit indicates an interrupt due to the reception of a packet exceeding the programmable maximum packet length. This interrupt can be masked using MAXLE.

MINLI:

The MINLI bit indicates an interrupt due to the reception of a packet that is smaller than the programmable minimum packet length. This interrupt can be masked using MINLE.

Register 0x0A3: RXFP Minimum Packet Length

Bit	Type	Function	Default
Bit 7	R/W	MINPL[7]	0
Bit 6	R/W	MINPL[6]	0
Bit 5	R/W	MINPL[5]	0
Bit 4	R/W	MINPL[4]	0
Bit 3	R/W	MINPL[3]	0
Bit 2	R/W	MINPL[2]	1
Bit 1	R/W	MINPL[1]	0
Bit 0	R/W	MINPL[0]	0

MINPL[7:0]:

The Minimum Packet Length (MINPL[7:0]) bits are used to set the minimum packet length. Packets smaller than this length are marked with an error. The packet length used here is defined as the number of bytes encapsulated into the POS frame, excluding byte stuffing and FCS bytes.

The minimum packet length supported by the RXFP is 3 bytes (0x03).

Register 0x0A4: RXFP Maximum Packet Length LSB

Bit	Type	Function	Default
Bit 7	R/W	MAXPL[7]	0
Bit 6	R/W	MAXPL[6]	0
Bit 5	R/W	MAXPL[5]	0
Bit 4	R/W	MAXPL[4]	0
Bit 3	R/W	MAXPL[3]	0
Bit 2	R/W	MAXPL[2]	0
Bit 1	R/W	MAXPL[1]	0
Bit 0	R/W	MAXPL[0]	0

Register 0x0A5: RXFP Maximum Packet Length MSB

Bit	Type	Function	Default
Bit 7	R/W	MAXPL[15]	0
Bit 6	R/W	MAXPL[14]	0
Bit 5	R/W	MAXPL[13]	0
Bit 4	R/W	MAXPL[12]	0
Bit 3	R/W	MAXPL[11]	0
Bit 2	R/W	MAXPL[10]	1
Bit 1	R/W	MAXPL[9]	1
Bit 0	R/W	MAXPL[8]	0

MAXPL[15:0]:

The Maximum Packet Length (MAXPL[15:0]) bits are used to set the maximum packet length. Packets larger than this length are marked with an error. The packet length used here is defined as the number of bytes encapsulated into the POS frame, excluding byte stuffing and FCS bytes.

The maximum packet length supported by the RXFP is 65534 bytes (0xFFFE).

Register 0x0A6: RXFP Receive Initiation Level

Bit	Type	Function	Default
Bit 7	R/W	Reserved	1
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	RIL[3]	1
Bit 2	R/W	RIL[2]	1
Bit 1	R/W	RIL[1]	0
Bit 0	R/W	RIL[0]	0

RIL[3:0]:

The Reception Initiation Level (RIL[3:0]) bits are used to set the minimum number of bytes that must be available in the FIFO before received packets can be written into it. RIL[3:0] is only used after a FIFO overrun has been detected and FIFO writes have been suspended. This avoids restarting the reception of data too quickly after an overrun condition. If the system does not cause any FIFO overrun, then this register will not be used. RIL[3:0] breaks the FIFO in 16 sections; for example a value of 0x4 correspond to a FIFO level of 64 bytes. The value of RIL must not be too large in order to prevent repetitive FIFO overruns and must not be programmed to zero.

Table 9 Receive Initiation Level Values

RIL[3:0]	FIFO Fill Level	RIL[3:0]	FIFO Fill Level
0000	0	1000	128
0001	16	1001	144
0010	32	1010	160
0011	48	1011	176
0100	64	1100	192
0101	80	1101	208
0110	96	1110	224
0111	112	1111	240

Register 0x0A7: RXFP Receive Packet Available High Water Mark

Bit	Type	Function	Default
Bit 7	R/W	RPAHWM[7]	0
Bit 6	R/W	RPAHWM[6]	1
Bit 5	R/W	RPAHWM[5]	0
Bit 4	R/W	RPAHWM[4]	0
Bit 3	R/W	RPAHWM[3]	0
Bit 2	R/W	RPAHWM[2]	0
Bit 1	R/W	RPAHWM[1]	0
Bit 0	R/W	RPAHWM[0]	0

RPAHWM[7:0]:

The Receive FIFO High Water Mark (RPAHWM[7:0]) bits are used to generate the RPA output in POS-PHY Level 2 interface. RPA is set to logic one when the number of bytes stored in the FIFO exceeds RPAHWM[7:0] or when there is at least one end of packet in the FIFO. The RPAHWM value is used to determine when data is transferred on the POS-PHY Level 2 interface.

The programmed value for RPAHWM[7:0] must be less than 0xF0 and greater than 0x00 for proper operation.

When a packet with less than 6 bytes arrives (from the line side), the receive packet available signal (RPA) may assert before data is available. In this condition, RPA will assert between 1 to 3 RFCLK clock cycles before the data is available and will remain asserted for 1 to 3 RFCLK clock cycles. When the Link Layer device attempts to read the packet by asserting read enable (RENB), it may find that there is no valid data available (receive data valid signal (RVAL) remains de-asserted). RPA will correctly assert again later when data is available. At this time the RVAL signal will be asserted indicating valid data.

With packets greater than 6 bytes, the RPA signal will assert, de-assert and then reassert 1 to 3 RFCLK cycles later (same as the above case with packets less than 6 bytes). However, if the Link layer device attempts to read the packet on the basis of the first occurrence of RPA, it will read valid data (RVAL will be asserted), even if RPA may be de-asserted.

This early assertion of RPA will not cause any data corruption if RVAL is used to qualify the data that is read. It is recommended that RVAL always be used to qualify receive data. The operation of RPA may cause a slight reduction of bandwidth on receive side of the POS-PHY interface. However, since there is ample bandwidth on the POS-PHY interface there will be no impact on performance of functionality.

Register 0x0A8: RXFP Receive Byte Count LSB

Bit	Type	Function	Default
Bit 7	R	RBYTE[7]	X
Bit 6	R	RBYTE[6]	X
Bit 5	R	RBYTE[5]	X
Bit 4	R	RBYTE[4]	X
Bit 3	R	RBYTE[3]	X
Bit 2	R	RBYTE[2]	X
Bit 1	R	RBYTE[1]	X
Bit 0	R	RBYTE[0]	X

Register 0x0A9: RXFP Receive Byte Count

Bit	Type	Function	Default
Bit 7	R	RBYTE[15]	X
Bit 6	R	RBYTE[14]	X
Bit 5	R	RBYTE[13]	X
Bit 4	R	RBYTE[12]	X
Bit 3	R	RBYTE[11]	X
Bit 2	R	RBYTE[10]	X
Bit 1	R	RBYTE[9]	X
Bit 0	R	RBYTE[8]	X

Register 0x0AA: RXFP Receive Byte Count

Bit	Type	Function	Default
Bit 7	R	RBYTE[23]	X
Bit 6	R	RBYTE[22]	X
Bit 5	R	RBYTE[21]	X
Bit 4	R	RBYTE[20]	X
Bit 3	R	RBYTE[19]	X
Bit 2	R	RBYTE[18]	X
Bit 1	R	RBYTE[17]	X
Bit 0	R	RBYTE[16]	X

Register 0x0AB: RXFP Receive Byte Count MSB

Bit	Type	Function	Default
Bit 7	R	RBYTE[31]	X
Bit 6	R	RBYTE[30]	X
Bit 5	R	RBYTE[29]	X
Bit 4	R	RBYTE[28]	X
Bit 3	R	RBYTE[27]	X
Bit 2	R	RBYTE[26]	X
Bit 1	R	RBYTE[25]	X
Bit 0	R	RBYTE[24]	X

RBYTE[31:0]:

The RBYTE[31:0] bits indicate the number of bytes received during the last accumulation interval. A write to any one of the RXFP Receive Byte Counter registers loads the registers with the current counter value and resets the internal counter to zero.

The count can also be polled by writing to the S/UNI-1x155 Master Reset and Identity register (0x000). Writing to register address 0x000 loads all counter registers in the channel and APS link.

The count can also be polled by writing to the channel Master Interrupt Status register (0x007). Writing to register 0x007 loads all counter registers in the RSOP, RLOP, RPOP, SPTB, SSTB, RXCP, TXCP, RXFP, and TXFP blocks of the channel.

Register 0x0AC: RXFP Receive Frame Count LSB

Bit	Type	Function	Default
Bit 7	R	RFRAME[7]	X
Bit 6	R	RFRAME[6]	X
Bit 5	R	RFRAME[5]	X
Bit 4	R	RFRAME[4]	X
Bit 3	R	RFRAME[3]	X
Bit 2	R	RFRAME[2]	X
Bit 1	R	RFRAME[1]	X
Bit 0	R	RFRAME[0]	X

Register 0x0AD: RXFP Receive Frame Count

Bit	Type	Function	Default
Bit 7	R	RFRAME[15]	X
Bit 6	R	RFRAME[14]	X
Bit 5	R	RFRAME[13]	X
Bit 4	R	RFRAME[12]	X
Bit 3	R	RFRAME[11]	X
Bit 2	R	RFRAME[10]	X
Bit 1	R	RFRAME[9]	X
Bit 0	R	RFRAME[8]	X

Register 0x0AE: RXFP Receive Frame Count MSB

Bit	Type	Function	Default
Bit 7	R	RFRAME[23]	X
Bit 6	R	RFRAME[22]	X
Bit 5	R	RFRAME[21]	X
Bit 4	R	RFRAME[20]	X
Bit 3	R	RFRAME[19]	X
Bit 2	R	RFRAME[18]	X
Bit 1	R	RFRAME[17]	X
Bit 0	R	RFRAME[16]	X

RFRAME[23:0]:

The RFRAME[23:0] bits indicate the number of received POS frames during the last accumulation interval. A write to any one of the RXFP Receive Frame Counter registers loads the registers with the current counter value and resets the internal counter to zero. To determine the number of packets that have been written into the FIFO, the RCNT registers may be used.

The count can also be polled by writing to the S/UNI-1x155 Master Reset and Identity register (0x000). Writing to register address 0x000 loads all counter registers in the channel and APS link.

The count can also be polled by writing to the channel Master Interrupt Status register (0x007). Writing to register 0x007 loads all counter registers in the RSOP, RLOP, RPOP, SPTB, SSTB, RXCP, TXCP, RXFP, and TXFP blocks of the channel.

Register 0x0AF: RXFP Receive Aborted Frame Count LSB

Bit	Type	Function	Default
Bit 7	R	RABRF[7]	X
Bit 6	R	RABRF[6]	X
Bit 5	R	RABRF[5]	X
Bit 4	R	RABRF[4]	X
Bit 3	R	RABRF[3]	X
Bit 2	R	RABRF[2]	X
Bit 1	R	RABRF[1]	X
Bit 0	R	RABRF[0]	X

Register 0x0B0: RXFP Receive Aborted Frame Count MSB

Bit	Type	Function	Default
Bit 7	R	RABRF[15]	X
Bit 6	R	RABRF[14]	X
Bit 5	R	RABRF[13]	X
Bit 4	R	RABRF[12]	X
Bit 3	R	RABRF[11]	X
Bit 2	R	RABRF[10]	X
Bit 1	R	RABRF[9]	X
Bit 0	R	RABRF[8]	X

RABRF[15:0]:

The RABRF[15:0] bits indicate the number of aborted POS frames received during the last accumulation interval. A write to any one of the RXFP Receive Aborted Frame Counter registers loads the registers with the current counter value and resets the internal counter to zero.

The count can also be polled by writing to the S/UNI-1x155 Master Reset and Identity register (0x000). Writing to register address 0x000 loads all counter registers in the channel and APS link.

The count can also be polled by writing to the channel Master Interrupt Status register (0x007). Writing to register 0x007 loads all counter registers in the RSOP, RLOP, RPOP, SPTB, SSTB, RXCP, TXCP, RXFP, and TXFP blocks of the channel.

Register 0x0B1: RXFP Receive FCS Error Frame Count LSB

Bit	Type	Function	Default
Bit 7	R	RFCSEF[7]	X
Bit 6	R	RFCSEF[6]	X
Bit 5	R	RFCSEF[5]	X
Bit 4	R	RFCSEF[4]	X
Bit 3	R	RFCSEF[3]	X
Bit 2	R	RFCSEF[2]	X
Bit 1	R	RFCSEF[1]	X
Bit 0	R	RFCSEF[0]	X

Register 0x0B2: RXFP Receive FCS Error Frame Count MSB

Bit	Type	Function	Default
Bit 7	R	RFCSEF[15]	X
Bit 6	R	RFCSEF[14]	X
Bit 5	R	RFCSEF[13]	X
Bit 4	R	RFCSEF[12]	X
Bit 3	R	RFCSEF[11]	X
Bit 2	R	RFCSEF[10]	X
Bit 1	R	RFCSEF[9]	X
Bit 0	R	RFCSEF[8]	X

RFCSEF[15:0]:

The RFCSEF[15:0] bits indicate the number of POS frames received with an FCS error during the last accumulation interval. A write to any one of the RXFP Receive FCS Error Frame Counter registers loads the registers with the current counter value and resets the internal counter to zero.

The count can also be polled by writing to the S/UNI-1x155 Master Reset and Identity register (0x000). Writing to register address 0x000 loads all counter registers in the channel and APS link.

The count can also be polled by writing to the channel Master Interrupt Status register (0x007). Writing to register 0x007 loads all counter registers in the RSOP, RLOP, RPOP, SPTB, SSTB, RXCP, TXCP, RXFP, and TXFP blocks of the channel.

Register 0x0B3: RXFP Receive Minimum Length Error Frame Count LSB

Bit	Type	Function	Default
Bit 7	R	RMINLF[7]	X
Bit 6	R	RMINLF[6]	X
Bit 5	R	RMINLF[5]	X
Bit 4	R	RMINLF[4]	X
Bit 3	R	RMINLF[3]	X
Bit 2	R	RMINLF[2]	X
Bit 1	R	RMINLF[1]	X
Bit 0	R	RMINLF[0]	X

Register 0x0B4: RXFP Receive Minimum Length Error Frame Counter MSB

Bit	Type	Function	Default
Bit 7	R	RMINLF[15]	X
Bit 6	R	RMINLF[14]	X
Bit 5	R	RMINLF[13]	X
Bit 4	R	RMINLF[12]	X
Bit 3	R	RMINLF[11]	X
Bit 2	R	RMINLF[10]	X
Bit 1	R	RMINLF[9]	X
Bit 0	R	RMINLF[8]	X

RMINLF[15:0]:

The RMINLF[15:0] bits indicate the number of minimum packet length POS frames received during the last accumulation interval. A write to any one of the RXFP Minimum Length Error Frame Counter registers loads the registers with the current counter value and resets the internal counter to zero.

The count can also be polled by writing to the S/UNI-1x155 Master Reset and Identity register (0x000). Writing to register address 0x000 loads all counter registers in the channel and APS link.

The count can also be polled by writing to the channel Master Interrupt Status register (0x007). Writing to register 0x007 loads all counter registers in the RSOP, RLOP, RPOP, SPTB, SSTB, RXCP, TXCP, RXFP, and TXFP blocks of the channel.

Register 0x0B5: RXFP Receive Maximum Length Error Frame Counter LSB

Bit	Type	Function	Default
Bit 7	R	RMAXLF[7]	X
Bit 6	R	RMAXLF[6]	X
Bit 5	R	RMAXLF[5]	X
Bit 4	R	RMAXLF[4]	X
Bit 3	R	RMAXLF[3]	X
Bit 2	R	RMAXLF[2]	X
Bit 1	R	RMAXLF[1]	X
Bit 0	R	RMAXLF[0]	X

Register 0x0B6: RXFP Receive Maximum Length Error Frame Counter MSB

Bit	Type	Function	Default
Bit 7	R	RMAXLF[15]	X
Bit 6	R	RMAXLF[14]	X
Bit 5	R	RMAXLF[13]	X
Bit 4	R	RMAXLF[12]	X
Bit 3	R	RMAXLF[11]	X
Bit 2	R	RMAXLF[10]	X
Bit 1	R	RMAXLF[9]	X
Bit 0	R	RMAXLF[8]	X

RMAXLF[15:0]:

The RMAXLF[15:0] bits indicate the number of POS frames exceeding the maximum packet length that were received during the last accumulation interval. A write to any one of the RXFP Receive Maximum Length Error Frame Counter registers loads the registers with the current counter value and resets the internal counter to zero.

The count can also be polled by writing to the S/UNI-1x155 Master Reset and Identity register (0x000). Writing to register address 0x000 loads all counter registers in the channel and APS link.

The count can also be polled by writing to the channel Master Interrupt Status register (0x007). Writing to register 0x007 loads all counter registers in the RSOP, RLOP, RPOP, SPTB, SSTB, RXCP, TXCP, RXFP, and TXFP blocks of the channel.

Register 0x0C0: TXFP Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R	FIFOERR	X
Bit 5	R/W	FUDRE	0
Bit 4	R	FUDRI	X
Bit 3	R/W	FOVRE	0
Bit 2	R	FOVRI	X
Bit 1	R/W	TPRTYE	0
Bit 0	R	TPRTYI	X

TPRTYI:

The TPRTYI bit indicates if a parity error was detected on the TDAT system interface bus. When logic one, the TPRTYI bit indicates a parity error over the TDAT[15:0] bus. This bit is cleared when this register is read. Odd or even parity is selected using the TPTYP bit. If during a continual parity mismatch condition, TPRTYI is cleared, it will only re-asserted if the parity error disappears and appears again. For a continual parity mismatch TPRTYI will be asserted only once.

TPRTYE:

The TPRTYE bit enables transmit parity interrupts. When set to logic one, parity errors are indicated on INTB and TPRTYI. When set to logic zero, parity errors are indicated using bit TPRTYI, but are not indicated on output INTB.

FOVRI:

The FOVRI bit is set high when an attempt is made to write into the FIFO while it has already been filled-up. This is considered a system error. This bit is reset immediately after a read to this register.

FOVRE:

The FOVRE bit enables the generation of an interrupt due to an attempt to write the FIFO when it is already full. When FOVRE is set to logic one, the interrupt is enabled and causes FOVRI and an interrupt is asserted. When set to logic zero, FOVRI will be asserted but not INTB.

FUDRI:

The FUDRI bit is set high when the channel buffer underruns while reading a packet data from the buffer. This bit is reset immediately after a read to this register.

FUDRE:

The FUDRE bit enables the generation of an interrupt due to a channel buffer underrun. When FUDRE is set to logic one, the interrupt is enabled and causes FUDRI and the output INTB to be asserted. When set to logic zero, FUDRI will be asserted, but not INTB.

FIFOERR:

The FIFOERR bit is set high when a packet is not properly delineated by a RSOP and REOP pair on the system interface. If the FIFO sees two start of packet indications (RSOP high) or two end of packet indications (REOP high), the current packet is aborted and FIFOERR is set high. This bit is reset immediately after a read to this register.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x0C1: TXFP Configuration

Bit	Type	Function	Default
Bit 7	R/W	XOFF	0
Bit 6	R/W	TPAINV	0
Bit 5	R/W	FCSERR	0
Bit 4	R/W	FCSSEL[1]	1
Bit 3	R/W	FCSSEL[0]	0
Bit 2	R/W	TPTYP	0
Bit 1	R/W	DSCR	1
Bit 0	R/W	FIFORST	0

FIFORST:

The FIFORST bit is used to reset the 256-byte transmit channel buffer. When FIFORST is set to logic zero, the channel buffer operates normally. When FIFORST is set to logic one, the buffer is emptied of all octets (including the current packet being transmitted) and ignores writes. The buffer remains empty and continues to ignore writes until a logic zero is written to FIFORST. Flags are transmitted until a subsequent packet is written to the FIFO.

The FIFORST must be set high before the per-channel FIFO reset in the TFCLK DLL is asserted. The FIFORST must be set low after the per-channel FIFO reset in the TFCLK DLL is de-asserted.

DSCR:

The DSCR bit controls the scrambling of the POS frames. When DSCR is a logic one, scrambling is enabled. When DSCR is a logic zero, payload scrambling is disabled.

TPTYP:

The TPTYP bit selects even or odd parity for input TPRTY for Level 2 operation. When set to logic one, the TPRTY input must report even parity for the TDAT system interface bus. When set to logic zero, input TPRTY must report odd parity for the TDAT bus.

FCSSEL[1:0]:

The Frame Control Sequence select (FCSSEL[1:0]) bits control the FCS calculation according to the table below. The FCS is calculated over the whole packet data, before byte stuffing and scrambling.

FCSSEL[1:0]	FCS Operation
00	No FCS inserted
01	CRC-16.ISO-3309 (2 bytes)
10	CRC-32 (4 bytes)

11	Reserved

FCSERR:

The FCSERR bit controls the insertion of FCS errors for diagnostic purposes. When FCSERR is set to logic one, if FCS insertion is enabled, the FCS octets are inverted prior to insertion in the POS frame. When FCSERR is set low, the FCS is inserted normally.

TPAINV:

The TPAINV bit inverts the polarity of the TPA output signal for Level 2 operation. When TPAINV is a logic one, the polarity of TPA is inverted. When TPAINV is a logic zero, TPA operates normally.

XOFF:

The XOFF serves as a transmission enable bit. When XOFF is set to logic zero, POS frames are transmitted normally. When XOFF is set to logic one, the current frame being transmitted is completed and then POS frame transmission is suspended. When XOFF is asserted the FIFO still accepts data and can overflow. XOFF is provided to facilitate system debugging rather than flow control. This bit should not be changed on the fly for flow control purposes.

Register 0x0C2: TXFP Control

Bit	Type	Function	Default
Bit 7	R/W	IPGAP[3]	0
Bit 6	R/W	IPGAP[2]	0
Bit 5	R/W	IPGAP[1]	1
Bit 4	R/W	IPGAP[0]	0
Bit 3	R/W	TIL[3]	0
Bit 2	R/W	TIL[2]	1
Bit 1	R/W	TIL[1]	0
Bit 0	R/W	TIL[0]	0

TIL[3:0]:

The Transmit Initiation Level (TIL[3:0]) bits are used to determine when to initiate a POS frame transmission. After the channel buffer is emptied, data transmission starts only when either there is a complete packet or when the number of bytes stored in the channel buffer equals or exceeds the value of TIL[3:0] times 16.

Once initiated, the transmission will continue until the packet is transmitted or an underrun occurs. Before starting another packet, a complete packet must be in the channel buffer or the buffer fill level must exceed the level specified by TIL[3:0].

Table 10 Transmit Initiation Level Values

TIL[3:0]	FIFO Fill Level	TIL[3:0]	FIFO Fill Level
0000	0	1000	128
0001	16	1001	144
0010	32	1010	160
0011	48	1011	176
0100	64	1100	192
0101	80	1101	208
0110	96	1110	224
0111	112	1111	240

IPGAP[3:0]:

The Inter Packet Gaping (IPGAP[3:0]) bits are used to program the number of Flag Sequence characters inserted between each POS Frame. These bits can not be dynamically modified. The programmed value is encoded as indicated in Table 11.

Table 11 Inter Packet Gaping Values

IPGAP[3:0]	Number of Flag
0000	1
0001	2
0010	4
0011	8
0100	16
0101	32
0110	64
0111	128

IPGAP[3:0]	Number of Flag
1000	256
1001	512
1010	1024
1011	2048
1100	4096
1101	8192
1110	16384
1111	32768

Register 0x0C3: TXFP Transmit Packet Available Low Water Mark

Bit	Type	Function	Default
Bit 7	R/W	TPALWM[7]	0
Bit 6	R/W	TPALWM[6]	1
Bit 5	R/W	TPALWM[5]	0
Bit 4	R/W	TPALWM[4]	0
Bit 3	R/W	TPALWM[3]	0
Bit 2	R/W	TPALWM[2]	0
Bit 1	R/W	TPALWM[1]	0
Bit 0	R/W	TPALWM[0]	0

TPALWM[7:0]:

The Transmit FIFO Low Water Mark (TPALWM[7:0]) bits are used to generate the TPA output. TPALWM must not be programmed with a value less than 0x0F for proper operation. Due to internal pipeline delay, the TPA output may not assert until the FIFO level has dropped a maximum of 16 bytes below the value specified by TPALWM.

For Level 2 system interfaces, TPA is set to logic one when the number of bytes stored in the FIFO is lower than TPALWM[7:0].

Register 0x0C4: TXFP Transmit Packet Available High Water Mark

Bit	Type	Function	Default
Bit 7	R/W	TPAHWM[7]	1
Bit 6	R/W	TPAHWM[6]	1
Bit 5	R/W	TPAHWM[5]	1
Bit 4	R/W	TPAHWM[4]	1
Bit 3	R/W	TPAHWM[3]	1
Bit 2	R/W	TPAHWM[2]	0
Bit 1	R/W	TPAHWM[1]	0
Bit 0	R/W	TPAHWM[0]	0

TPAHWM[7:0]:

The Transmit FIFO High Water Mark (TPAHWM[7:0]) bits are used to generate the TPA output. TPAHWM must not be programmed with a value greater than 0xF0 for proper operation. Due to internal pipeline delay, the TPA output may not deassert until the FIFO level has raised a maximum of 8 bytes above the value specified by TPAHWM.

For Level 2 system interfaces, TPA is set to logic zero when the number of bytes stored in the FIFO exceeds TPAHWM[7:0].

Register 0x0C5: TXFP Transmit Byte Count LSB

Bit	Type	Function	Default
Bit 7	R	TBYTE[7]	X
Bit 6	R	TBYTE[6]	X
Bit 5	R	TBYTE[5]	X
Bit 4	R	TBYTE[4]	X
Bit 3	R	TBYTE[3]	X
Bit 2	R	TBYTE[2]	X
Bit 1	R	TBYTE[1]	X
Bit 0	R	TBYTE[0]	X

Register 0x0C6: TXFP Transmit Byte Count

Bit	Type	Function	Default
Bit 7	R	TBYTE[15]	X
Bit 6	R	TBYTE[14]	X
Bit 5	R	TBYTE[13]	X
Bit 4	R	TBYTE[12]	X
Bit 3	R	TBYTE[11]	X
Bit 2	R	TBYTE[10]	X
Bit 1	R	TBYTE[9]	X
Bit 0	R	TBYTE[8]	X

Register 0x0C7: TXFP Transmit Byte Count

Bit	Type	Function	Default
Bit 7	R	TBYTE[23]	X
Bit 6	R	TBYTE[22]	X
Bit 5	R	TBYTE[21]	X
Bit 4	R	TBYTE[20]	X
Bit 3	R	TBYTE[19]	X
Bit 2	R	TBYTE[18]	X
Bit 1	R	TBYTE[17]	X
Bit 0	R	TBYTE[16]	X

Register 0x0C8: TXFP Transmit Byte Count MSB

Bit	Type	Function	Default
Bit 7	R	TBYTE[31]	X
Bit 6	R	TBYTE[30]	X
Bit 5	R	TBYTE[29]	X
Bit 4	R	TBYTE[28]	X
Bit 3	R	TBYTE[27]	X
Bit 2	R	TBYTE[26]	X
Bit 1	R	TBYTE[25]	X
Bit 0	R	TBYTE[24]	X

TBYTE[31:0]:

The TBYTE[31:0] bits indicate the number of bytes read from the transmit FIFO and transmitted during the last accumulation interval. This counter does not count bytes within aborted frames. A write to any one of the TXFP Transmit Byte Counter registers loads the registers with the current counter value and resets the internal counter to zero.

The count can also be polled by writing to the S/UNI-1x155 Master Reset and Identity register (0x000). Writing to register address 0x000 loads all counter registers in the channel and APS link.

The count can also be polled by writing to the channel Master Interrupt Status register (0x007). Writing to register 0x007 loads all counter registers in the RSOP, RLOP, RPOP, SPTB, SSTB, RXCP, TXCP, RXFP, and TXFP blocks of the channel.

Register 0x0C9: TXFP Transmit Frame Count LSB

Bit	Type	Function	Default
Bit 7	R	TFRAME[7]	X
Bit 6	R	TFRAME[6]	X
Bit 5	R	TFRAME[5]	X
Bit 4	R	TFRAME[4]	X
Bit 3	R	TFRAME[3]	X
Bit 2	R	TFRAME[2]	X
Bit 1	R	TFRAME[1]	X
Bit 0	R	TFRAME[0]	X

Register 0x0CA: TXFP Transmit Frame Count

Bit	Type	Function	Default
Bit 7	R	TFRAME[15]	X
Bit 6	R	TFRAME[14]	X
Bit 5	R	TFRAME[13]	X
Bit 4	R	TFRAME[12]	X
Bit 3	R	TFRAME[11]	X
Bit 2	R	TFRAME[10]	X
Bit 1	R	TFRAME[9]	X
Bit 0	R	TFRAME[8]	X

Register 0x0CB: TXFP Transmit Frame Count MSB

Bit	Type	Function	Default
Bit 7	R	TFRAME[23]	X
Bit 6	R	TFRAME[22]	X
Bit 5	R	TFRAME[21]	X
Bit 4	R	TFRAME[20]	X
Bit 3	R	TFRAME[19]	X
Bit 2	R	TFRAME[18]	X
Bit 1	R	TFRAME[17]	X
Bit 0	R	TFRAME[16]	X

TFRAME[23:0]:

The TFRAME[23:0] bits indicate the number of POS frames read from the transmit FIFO and inserted into the transmission stream during the last accumulation interval. This counter does not count aborted frames. A write to any one of the TXFP Transmit Frame Counter registers loads the registers with the current counter value and resets the internal counter to zero.

The count can also be polled by writing to the S/UNI-1x155 Master Reset and Identity register (0x000). Writing to register address 0x000 loads all counter registers in the channel and APS link.

The count can also be polled by writing to the channel Master Interrupt Status register (0x007). Writing to register 0x007 loads all counter registers in the RSOP, RLOP, RPOP, SPTB, SSTB, RXCP, TXCP, RXFP, and TXFP blocks of the channel.

Register 0x0CC: TXFP Transmit User Aborted Frame Count LSB

Bit	Type	Function	Default
Bit 7	R	TUSRABF[7]	X
Bit 6	R	TUSRABF[6]	X
Bit 5	R	TUSRABF[5]	X
Bit 4	R	TUSRABF[4]	X
Bit 3	R	TUSRABF[3]	X
Bit 2	R	TUSRABF[2]	X
Bit 1	R	TUSRABF[1]	X
Bit 0	R	TUSRABF[0]	X

Register 0x0CD: TXFP Transmit User Aborted Frame Count MSB

Bit	Type	Function	Default
Bit 7	R	TUSRABF[15]	X
Bit 6	R	TUSRABF[14]	X
Bit 5	R	TUSRABF[13]	X
Bit 4	R	TUSRABF[12]	X
Bit 3	R	TUSRABF[11]	X
Bit 2	R	TUSRABF[10]	X
Bit 1	R	TUSRABF[9]	X
Bit 0	R	TUSRABF[8]	X

TUSRABF[15:0]:

The TUSRABF[15:0] bits indicate the number of user aborted POS frames read from the transmit FIFO and inserted into the transmission stream during the last accumulation interval. User can abort frames by asserting TERR. A write to any one of the TXFP Transmit User Aborted Frame Counter registers loads the registers with the current counter value and resets the internal counter to zero.

The count can also be polled by writing to the S/UNI-1x155 Master Reset and Identity register (0x000). Writing to register address 0x000 loads all counter registers in the channel and APS link.

The count can also be polled by writing to the channel Master Interrupt Status register (0x007). Writing to register 0x007 loads all counter registers in the RSOP, RLOP, RPOP, SPTB, SSTB, RXCP, TXCP, RXFP, and TXFP blocks of the channel.

Register 0x0CE: TXFP Transmit Underrun/Error Aborted Frame Count LSB

Bit	Type	Function	Default
Bit 7	R	TFERABF[7]	X
Bit 6	R	TFERABF[6]	X
Bit 5	R	TFERABF[5]	X
Bit 4	R	TFERABF[4]	X
Bit 3	R	TFERABF[3]	X
Bit 2	R	TFERABF[2]	X
Bit 1	R	TFERABF[1]	X
Bit 0	R	TFERABF[0]	X

Register 0x0CF: TXFP Transmit Underrun/Error Aborted Frame Count MSB

Bit	Type	Function	Default
Bit 7	R	TFERABF[15]	X
Bit 6	R	TFERABF[14]	X
Bit 5	R	TFERABF[13]	X
Bit 4	R	TFERABF[12]	X
Bit 3	R	TFERABF[11]	X
Bit 2	R	TFERABF[10]	X
Bit 1	R	TFERABF[9]	X
Bit 0	R	TFERABF[8]	X

TFERABF[15:0]:

The TFERABF[15:0] bits indicate the number of FIFO underrun error aborted POS frames read from the transmit FIFO and inserted into the transmission stream during the last accumulation interval. FIFO underruns errors are caused when the FIFO runs empty and the last byte read was not an end of packet or also when the FIFO overruns and corrupts the end of packet/start of packet sequence (example: when another RSOP is high when expecting an REOP). This is considered a system error and should not occur when the system works normally. A write to any one of the TXFP Transmit User Aborted Frame Counter registers loads the registers with the current counter value and resets the internal counter to zero.

The count can also be polled by writing to the S/UNI-1x155 Master Reset and Identity register (0x000). Writing to register address 0x000 loads all counter registers in the channel and APS link.

The count can also be polled by writing to the channel Master Interrupt Status register (0x007). Writing to register 0x007 loads all counter registers in the RSOP, RLOP, RPOP, SPTB, SSTB, RXCP, TXCP, RXFP, and TXFP blocks of the channel.

Register 0x0D0: WANS Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	FORCEREAC	0
Bit 2	R/W	AUTOREAC	0
Bit 1	R/W	INTEN	0
Bit 0	R/W	PHACOMPEN	0

PHACOMPEN:

The Phase Comparison Enable (PHACOMPEN) bit is used to enable the phase comparison process. Setting this bit to a logic one will enable the phase comparison process. When set low, the phase and reference period counters are kept in reset state, further disabling the WANS process

INTEN:

The Interrupt Enable (INTEN) bit controls the generation of the interrupt signal. When set high, this bit allows the generation of an interrupt signal at the beginning of the Phase Detector averaging period. Setting this bit to logic zero disables the generation of the interrupts.

AUTOREAC:

The Auto Reacquisition Mode Select (AUTOREAC) bit can be used to set the WANS to automatic phase reacquisition mode. When operating in this mode, the WANS will automatically align the phase sampling point toward the middle of the Phase Counter period upon detection of two consecutive Phase Sample located on each side of the Phase Counter wrap around value. The Phase Word register will keep its previous value till. Setting this bit to logic one enables the automatic reacquisition mode.

FORCEREAC:

The Force Phase Reacquisition (FORCEREAC) bit can be used to force a phase reacquisition of the Phase Detector. A logic zero to logic one transition on this bit triggers a phase reacquisition sequence of the Phase Detector. Setting this bit to logic zero allows the Phase detector to operate normally.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x0D1: WANS Interrupt and Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	RPHALGN	X
Bit 0	R	TIMI	X

TIMI:

The Timer Interrupt (TIMI) bit indicates a Timer Interrupt condition. This bit will be raised at the beginning of the Phase Detector averaging period. In addition to indicating the interrupt status, this bit can also be polled to synchronize read access to the WANS output register. This interrupt can be masked using the INTEN bit of the configuration register. A read access to the Interrupt & Status Register resets the value of this bit.

RPHALGN:

The Reference Phase Alignment (RPHALNG) bit indicates a Reference Phase Alignment event. In normal operating mode, this bit remains set to logic zero. Upon the occurrence of a Reference Phase Alignment, this bit is set to logic one, indicating that the phase averaging process was aborted and that the value of the Phase Word register is frozen to the previous valid value. This bit is reset low after the completion of a valid phase averaging cycle.

Register 0x0D2: WANS Phase Word LSB

Bit	Type	Function	Default
Bit 7	R	PHAWORD[7]	X
Bit 6	R	PHAWORD[6]	X
Bit 5	R	PHAWORD[5]	X
Bit 4	R	PHAWORD[4]	X
Bit 3	R	PHAWORD[3]	X
Bit 2	R	PHAWORD[2]	X
Bit 1	R	PHAWORD[1]	X
Bit 0	R	PHAWORD[0]	X

Register 0x0D3: WANS Phase Word

Bit	Type	Function	Default
Bit 7	R	PHAWORD[15]	X
Bit 6	R	PHAWORD[14]	X
Bit 5	R	PHAWORD[13]	X
Bit 4	R	PHAWORD[12]	X
Bit 3	R	PHAWORD[11]	X
Bit 2	R	PHAWORD[10]	X
Bit 1	R	PHAWORD[9]	X
Bit 0	R	PHAWORD[8]	X

Register 0x0D4: WANS Phase Word

Bit	Type	Function	Default
Bit 7	R	PHAWORD[23]	X
Bit 6	R	PHAWORD[22]	X
Bit 5	R	PHAWORD[21]	X
Bit 4	R	PHAWORD[20]	X
Bit 3	R	PHAWORD[19]	X
Bit 2	R	PHAWORD[18]	X
Bit 1	R	PHAWORD[17]	X
Bit 0	R	PHAWORD[16]	X

Register 0x0D5: WANS Phase Word MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	PHAWORD[30]	X
Bit 5	R	PHAWORD[29]	X
Bit 4	R	PHAWORD[28]	X
Bit 3	R	PHAWORD[27]	X
Bit 2	R	PHAWORD[26]	X
Bit 1	R	PHAWORD[25]	X
Bit 0	R	PHAWORD[24]	X

PHAWORD[30:0]:

The Phase Word (PHAWORD[30:0]) bits are the output bus of the Phase Detector. This bus outputs the result of the Phase Count Averaging function. Depending on the number of samples included in the averaging, from 0 to 15 of the LSB(s) of the PHAWORD bus may represent the fractional part of the average value while the 16 following bits hold the integer part. This value can be used to externally implement in software the PLL filtering function and bypass the Digital Loop Filter block.

Register 0x0D9: WANS Reference Period LSB

Bit	Type	Function	Default
Bit 7	R/W	REFPER[7]	0
Bit 6	R/W	REFPER[6]	0
Bit 5	R/W	REFPER[5]	0
Bit 4	R/W	REFPER[4]	0
Bit 3	R/W	REFPER[3]	0
Bit 2	R/W	REFPER[2]	0
Bit 1	R/W	REFPER[1]	0
Bit 0	R/W	REFPER[0]	0

Register 0x0DA: WANS Reference Period MSB

Bit	Type	Function	Default
Bit 7	R/W	REFPER[15]	0
Bit 6	R/W	REFPER[14]	0
Bit 5	R/W	REFPER[13]	0
Bit 4	R/W	REFPER[12]	0
Bit 3	R/W	REFPER[11]	0
Bit 2	R/W	REFPER[10]	0
Bit 1	R/W	REFPER[9]	0
Bit 0	R/W	REFPER[8]	0

REFPER[15:0]:

The Reference Period REFPER[15:0] bits are used to program the timing reference period of the Phase Detector. These bits are used to set the end of count of the Reference Period Counter. The Reference Period Counter is reset on the next clock cycle following the detection of its end of count. The Reference Period Counter counts (Nref) is equal to the REFPER value plus 1.

Register 0x0DB: WANS Phase Counter Period LSB

Bit	Type	Function	Default
Bit 7	R/W	PHCNTPER[7]	0
Bit 6	R/W	PHCNTPER[6]	0
Bit 5	R/W	PHCNTPER[5]	0
Bit 4	R/W	PHCNTPER[4]	0
Bit 3	R/W	PHCNTPER[3]	0
Bit 2	R/W	PHCNTPER[2]	0
Bit 1	R/W	PHCNTPER[1]	0
Bit 0	R/W	PHCNTPER[0]	0

Register 0x0DC: WANS Phase Counter Period MSB

Bit	Type	Function	Default
Bit 7	R/W	PHCNTPER[15]	0
Bit 6	R/W	PHCNTPER[14]	0
Bit 5	R/W	PHCNTPER[13]	0
Bit 4	R/W	PHCNTPER[12]	0
Bit 3	R/W	PHCNTPER[11]	0
Bit 2	R/W	PHCNTPER[10]	0
Bit 1	R/W	PHCNTPER[9]	0
Bit 0	R/W	PHCNTPER[8]	0

PHCNTPER[15:0]:

The Phase Counter Period (PHCNTPER15:0]) bits are used to program the Phase Counter period of the Phase Detector. These bits are used to set the end of count of the Phase Counter. The Phase Counter is reset on the next clock cycle following the detection of its end of count. The Phase Counter count (Nphcnt) is equal to the PHCNTPER value plus 1.

For the system to operate properly, Nphcnt need to be greater than 1023.

Register 0x0DD: WANS Phase Average Period

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	PHAVGPER[3]	0
Bit 2	R/W	PHAVGPER[2]	0
Bit 1	R/W	PHAVGPER[1]	0
Bit 0	R/W	PHAVGPER[0]	0

PHAVGPER[3:0]:

The Phase Average Period (PHAVGPER [3:0]) bits are used to set the number of consecutive valid Phase Samples accumulated to form the Phase Word. The number of samples is expressed as a power of 2, i.e.:

$$N_{AVG} = 2^{PHAVGPER}$$

Register 0x0E0: RASE Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	PSBFE	0
Bit 6	R/W	COAPSE	0
Bit 5	R/W	Z1/S1E	0
Bit 4	R/W	SFBERE	0
Bit 3	R/W	SDBERE	0
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

SDBERE:

The SDBERE bit is the interrupt enable for the signal degrade threshold alarm. When SDBERE is a logic one, an interrupt is generated when the SD alarm is declared or removed.

SFBERE:

The SFBERE bit is the interrupt enable for the signal fail threshold alarm. When SFBERE is a logic one, an interrupt is generated when the SF alarm is declared or removed.

Z1/S1E:

The Z1/S1 interrupt enable is an interrupt mask for changes in the received synchronization status. When Z1/S1E is a logic one, an interrupt is generated when a new synchronization status message is extracted into the Receive Z1/S1 register.

COAPSE:

The COAPS interrupt enable is an interrupt mask for changes in the received APS code. When COAPSE is a logic one, an interrupt is generated when a new K1/K2 code value is extracted into the RASE Receive K1 and RASE Receive K2 registers.

PSBFE:

The PSBF interrupt enable is an interrupt mask for protection switch byte failure alarms. When PSBFE is a logic one, an interrupt is generated when PSBF is declared or removed.

Register 0x0E1: RASE Interrupt Status

Bit	Type	Function	Default
Bit 7	R	PSBFI	X
Bit 6	R	COAPSI	X
Bit 5	R	Z1/S1I	X
Bit 4	R	SFBERI	X
Bit 3	R	SDBERI	X
Bit 2	R	SFBERV	X
Bit 1	R	SDBERV	X
Bit 0	R	PSBFV	X

PSBFV:

The PSBFV bit indicates the protection switching byte failure alarm state. The alarm is declared (PSBFV is set high) when twelve successive frames have been received without three consecutive frames containing identical K1 bytes. The alarm is removed (PSBFV is set low) when three consecutive frames containing identical K1 bytes have been received.

SDBERV:

The SDBERV bit indicates the signal degrade threshold crossing alarm state. The alarm is declared (SDBERV is set high) when the bit error rate exceeds the threshold programmed in the RASE SD Declaring Threshold registers. The alarm is removed (SDBERV is set low) when the bit error rate is below the threshold programmed in the RASE SD Clearing Threshold registers.

SFBERV:

The SFBERV bit indicates the signal failure threshold crossing alarm state. The alarm is declared (SFBERV is set high) when the bit error rate exceeds the threshold programmed in the RASE SF Declaring Threshold registers. The alarm is removed (SFBERV is set low) when the bit error rate is below the threshold programmed in the RASE SF Clearing Threshold registers.

SDBERI:

The SDBERI bit is set high when the signal degrade threshold crossing alarm is declared or removed. This bit is cleared when the RASE Interrupt Status register is read.

SFBERI:

The SFBERI bit is set high when the signal failure threshold crossing alarm is declared or removed. This bit is cleared when the RASE Interrupt Status register is read.

Z1/S1I:

The Z1/S1I bit is set high when a new synchronization status message has been extracted into the RASE Receive Z1/S1 register. This bit is cleared when the RASE Interrupt Status register is read.

COAPSI:

The COAPSI bit is set high when a new APS code value has been extracted into the RASE Receive K1 and RASE Receive K2 registers. This bit is cleared when the RASE Interrupt Status register is read.

PSBFI:

The PSBFI bit is set high when the protection switching byte failure alarm is declared or removed. This bit is cleared when the RASE Interrupt Status register is read.

Register 0x0E2: RASE Configuration/Control

Bit	Type	Function	Default
Bit 7	R/W	Z1/S1_CAP	0
Bit 6	R/W	SFBERTEN	0
Bit 5	R/W	SFSMODE	0
Bit 4	R/W	SFCMODE	0
Bit 3	R/W	SDBERTEN	0
Bit 2	R/W	SDSMODE	0
Bit 1	R/W	SDCMODE	0
Bit 0	R/W	Reserved	0

SDCMODE:

The SDCMODE alarm bit selects the RASE window size to use for clearing the SD alarm. When SDCMODE is a logic zero the RASE clears the SD alarm using the same window size used for declaration. When SDCMODE is a logic one, the RASE clears the SD alarm using a window size that is 8 times longer than the alarm declaration window size. The declaration window size is determined by the RASE SD Accumulation Period registers.

SDSMODE:

The SDSMODE bit selects the RASE saturation mode. When SDSMODE is a logic zero the RASE limits the number of B2 errors accumulated in one frame period to the RASE SD Saturation Threshold register value. When SDSMODE is a logic one, the RASE limits the number of B2 errors accumulated in one window subtotal accumulation period to the RASE SD Saturation Threshold register value. Note that the number of frames in a window subtotal accumulation period is determined by the RASE SD Accumulation Period register value.

SDBERTEN:

The SDBERTEN bit selects automatic monitoring of line bit error rate threshold events by the RASE. When SDBERTEN is a logic one, the RASE continuously monitors line BIP errors over a period defined in the RASE configuration registers. When SDBERTEN is a logic zero, the RASE BIP accumulation logic is disabled, and the RASE logic is reset to the declaration monitoring state.

All RASE accumulation period and threshold registers should be set up before SDBERTEN is written.

SFCMODE:

The SFCMODE alarm bit selects the RASE window size to use for clearing the SF alarm. When SFCMODE is a logic zero the RASE clears the SF alarm using the same window size used for declaration. When SFCMODE is a logic one, the RASE clears the SF alarm using a window size that is 8 times longer than the alarm declaration window size. The declaration window size is determined by the RASE SF Accumulation Period registers.

SFSMODE:

The SFSMODE bit selects the RASE saturation mode. When SFSMODE is a logic zero the RASE limits the number of B2 errors accumulated in one frame period to the RASE SF Saturation Threshold register value. When SFSMODE is a logic one, the RASE limits the number of B2 errors accumulated in one window subtotal accumulation period to the RASE SF Saturation Threshold register value. Note that the number of frames in a window subtotal accumulation period is determined by the RASE SF Accumulation Period register value.

SFBERTEN:

The SFBERTEN bit enables automatic monitoring of line bit error rate threshold events by the RASE. When SFBERTEN is a logic one, the RASE continuously monitors line BIP errors over a period defined in the RASE configuration registers. When SFBERTEN is a logic zero, the RASE BIP accumulation logic is disabled, and the RASE logic is reset to the declaration monitoring state.

All RASE accumulation period and threshold registers should be set up before SFBERTEN is written.

Z1/S1_CAP:

The Z1/S1_CAP bit enables the Z1/S1 Capture algorithm. When Z1/S1_CAP is a logic one, the Z1/S1 clock synchronization status message nibble must have the same value for eight consecutive frames before writing the new value into the RASE Receive Z1/S1 register. When Z1/S1_CAP is logic zero, the Z1/S1 nibble value is written directly into the RASE Receive Z1/S1 register.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x0E3: RASE SF Accumulation Period LSB

Bit	Type	Function	Default
Bit 7	R/W	SFSAP[7]	0
Bit 6	R/W	SFSAP[6]	0
Bit 5	R/W	SFSAP[5]	0
Bit 4	R/W	SFSAP[4]	0
Bit 3	R/W	SFSAP[3]	0
Bit 2	R/W	SFSAP[2]	0
Bit 1	R/W	SFSAP[1]	0
Bit 0	R/W	SFSAP[0]	0

Register 0x0E4: RASE SF Accumulation Period

Bit	Type	Function	Default
Bit 7	R/W	SFSAP[15]	0
Bit 6	R/W	SFSAP[14]	0
Bit 5	R/W	SFSAP[13]	0
Bit 4	R/W	SFSAP[12]	0
Bit 3	R/W	SFSAP[11]	0
Bit 2	R/W	SFSAP[10]	0
Bit 1	R/W	SFSAP[9]	0
Bit 0	R/W	SFSAP[8]	0

Register 0x0E5: RASE SF Accumulation Period MSB

Bit	Type	Function	Default
Bit 7	R/W	SFSAP[23]	0
Bit 6	R/W	SFSAP[22]	0
Bit 5	R/W	SFSAP[21]	0
Bit 4	R/W	SFSAP[20]	0
Bit 3	R/W	SFSAP[19]	0
Bit 2	R/W	SFSAP[18]	0
Bit 1	R/W	SFSAP[17]	0
Bit 0	R/W	SFSAP[16]	0

SFSAP[23:0]:

The SFSAP[23:0] bits represent the number of 8 KHz frames used to accumulate the B2 error subtotal. The total evaluation window to declare the SF alarm is broken into 8 subtotals, so this register value represents 1/8 of the total sliding window size. Refer to the Operation section for recommended settings.

Register 0x0E6: RASE SF Saturation Threshold LSB

Bit	Type	Function	Default
Bit 7	R/W	SFSTH[7]	0
Bit 6	R/W	SFSTH[6]	0
Bit 5	R/W	SFSTH[5]	0
Bit 4	R/W	SFSTH[4]	0
Bit 3	R/W	SFSTH[3]	0
Bit 2	R/W	SFSTH[2]	0
Bit 1	R/W	SFSTH[1]	0
Bit 0	R/W	SFSTH[0]	0

Register 0x0E7: RASE SF Saturation Threshold MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	SFSTH[11]	0
Bit 2	R/W	SFSTH[10]	0
Bit 1	R/W	SFSTH[9]	0
Bit 0	R/W	SFSTH[8]	0

SFSTH[11:0]:

The SFSTH[11:0] value represents the allowable number of B2 errors that can be accumulated during an evaluation window before an SF threshold event is declared. Setting this threshold to 0xFFF disables the saturation functionality. Refer to the Operation section for the recommended settings.

Register 0x0E8: RASE SF Declaring Threshold LSB

Bit	Type	Function	Default
Bit 7	R/W	SFDTH[7]	0
Bit 6	R/W	SFDTH[6]	0
Bit 5	R/W	SFDTH[5]	0
Bit 4	R/W	SFDTH[4]	0
Bit 3	R/W	SFDTH[3]	0
Bit 2	R/W	SFDTH[2]	0
Bit 1	R/W	SFDTH[1]	0
Bit 0	R/W	SFDTH[0]	0

Register 0x0E9: RASE SF Declaring Threshold MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	SFDTH[11]	0
Bit 2	R/W	SFDTH[10]	0
Bit 1	R/W	SFDTH[9]	0
Bit 0	R/W	SFDTH[8]	0

SFDTH[11:0]:

The SFDTH[11:0] value determines the threshold for the declaration of the SF alarm. The SF alarm is declared when the number of B2 errors accumulated during an evaluation window is greater than or equal to the SFDTH[11:0] value. Refer to the Operation section for the recommended settings.

Register 0x0EA: RASE SF Clearing Threshold LSB

Bit	Type	Function	Default
Bit 7	R/W	SFCTH[7]	0
Bit 6	R/W	SFCTH[6]	0
Bit 5	R/W	SFCTH[5]	0
Bit 4	R/W	SFCTH[4]	0
Bit 3	R/W	SFCTH[3]	0
Bit 2	R/W	SFCTH[2]	0
Bit 1	R/W	SFCTH[1]	0
Bit 0	R/W	SFCTH[0]	0

Register 0x0EB: RASE SF Clearing Threshold MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	SFCTH[11]	0
Bit 2	R/W	SFCTH[10]	0
Bit 1	R/W	SFCTH[9]	0
Bit 0	R/W	SFCTH[8]	0

SFCTH[11:0]:

The SFCTH[11:0] value determines the threshold for the removal of the SF alarm. The SF alarm is removed when the number of B2 errors accumulated during an evaluation window is less than the SFCTH[11:0] value. Refer to the Operation section for the recommended settings.

Register 0x0EC: RASE SD Accumulation Period LSB

Bit	Type	Function	Default
Bit 7	R/W	SDSAP[7]	0
Bit 6	R/W	SDSAP[6]	0
Bit 5	R/W	SDSAP[5]	0
Bit 4	R/W	SDSAP[4]	0
Bit 3	R/W	SDSAP[3]	0
Bit 2	R/W	SDSAP[2]	0
Bit 1	R/W	SDSAP[1]	0
Bit 0	R/W	SDSAP[0]	0

Register 0x0ED: RASE SD Accumulation Period

Bit	Type	Function	Default
Bit 7	R/W	SDSAP[15]	0
Bit 6	R/W	SDSAP[14]	0
Bit 5	R/W	SDSAP[13]	0
Bit 4	R/W	SDSAP[12]	0
Bit 3	R/W	SDSAP[11]	0
Bit 2	R/W	SDSAP[10]	0
Bit 1	R/W	SDSAP[9]	0
Bit 0	R/W	SDSAP[8]	0

Register 0x0EE: RASE SD Accumulation Period MSB

Bit	Type	Function	Default
Bit 7	R/W	SDSAP[23]	0
Bit 6	R/W	SDSAP[22]	0
Bit 5	R/W	SDSAP[21]	0
Bit 4	R/W	SDSAP[20]	0
Bit 3	R/W	SDSAP[19]	0
Bit 2	R/W	SDSAP[18]	0
Bit 1	R/W	SDSAP[17]	0
Bit 0	R/W	SDSAP[16]	0

SDSAP[23:0]:

The SDSAP[23:0] bits represent the number of 8 KHz frames used to accumulate the B2 error subtotal. The total evaluation window to declare the SD alarm is broken into 8 subtotals, so this register value represents 1/8 of the total sliding window size. Refer to the Operation section for recommended settings.

Register 0x0EF: RASE SD Saturation Threshold LSB

Bit	Type	Function	Default
Bit 7	R/W	SDSTH[7]	0
Bit 6	R/W	SDSTH[6]	0
Bit 5	R/W	SDSTH[5]	0
Bit 4	R/W	SDSTH[4]	0
Bit 3	R/W	SDSTH[3]	0
Bit 2	R/W	SDSTH[2]	0
Bit 1	R/W	SDSTH[1]	0
Bit 0	R/W	SDSTH[0]	0

Register 0x0F0: RASE SD Saturation Threshold MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	SDSTH[11]	0
Bit 2	R/W	SDSTH[10]	0
Bit 1	R/W	SDSTH[9]	0
Bit 0	R/W	SDSTH[8]	0

SDSTH[11:0]:

The SDSTH[11:0] value represents the allowable number of B2 errors that can be accumulated during an evaluation window before an SD threshold event is declared. Setting this threshold to 0xFFF disables the saturation functionality. Refer to the Operation section for the recommended settings.

Register 0x0F1: RASE SD Declaring Threshold LSB

Bit	Type	Function	Default
Bit 7	R/W	SDDTH[7]	0
Bit 6	R/W	SDDTH[6]	0
Bit 5	R/W	SDDTH[5]	0
Bit 4	R/W	SDDTH[4]	0
Bit 3	R/W	SDDTH[3]	0
Bit 2	R/W	SDDTH[2]	0
Bit 1	R/W	SDDTH[1]	0
Bit 0	R/W	SDDTH[0]	0

Register 0x0F2: RASE SD Declaring Threshold MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	SDDTH[11]	0
Bit 2	R/W	SDDTH[10]	0
Bit 1	R/W	SDDTH[9]	0
Bit 0	R/W	SDDTH[8]	0

SDDTH[11:0]:

The SDDTH[11:0] value determines the threshold for the declaration of the SD alarm. The SD alarm is declared when the number of B2 errors accumulated during an evaluation window is greater than or equal to the SDDTH[11:0] value. Refer to the Operation section for the recommended settings.

Register 0x0F3: RASE SD Clearing Threshold LSB

Bit	Type	Function	Default
Bit 7	R/W	SDCTH[7]	0
Bit 6	R/W	SDCTH[6]	0
Bit 5	R/W	SDCTH[5]	0
Bit 4	R/W	SDCTH[4]	0
Bit 3	R/W	SDCTH[3]	0
Bit 2	R/W	SDCTH[2]	0
Bit 1	R/W	SDCTH[1]	0
Bit 0	R/W	SDCTH[0]	0

Register 0x0F4: RASE SD Clearing Threshold MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	SDCTH[11]	0
Bit 2	R/W	SDCTH[10]	0
Bit 1	R/W	SDCTH[9]	0
Bit 0	R/W	SDCTH[8]	0

SDCTH[11:0]:

The SDCTH[11:0] value determines the threshold for the removal of the SD alarm. The SD alarm is removed when the number of B2 errors accumulated during an evaluation window is less than the SDCTH[11:0] value. Refer to the Operation section for the recommended settings.

Register 0x0F5: RASE Receive K1

Bit	Type	Function	Default
Bit 7	R	K1[7]	X
Bit 6	R	K1[6]	X
Bit 5	R	K1[5]	X
Bit 4	R	K1[4]	X
Bit 3	R	K1[3]	X
Bit 2	R	K1[2]	X
Bit 1	R	K1[1]	X
Bit 0	R	K1[0]	X

K1[7:0]:

The K1[7:0] bits contain the current K1 code value. The contents of this register are updated when a new K1 code value (different from the current K1 code value) has been received for three consecutive frames. An interrupt may be generated when a new code value is received (using the COAPSE bit in the RASE Interrupt Enable Register). K1[7] is the most significant bit corresponding to bit 1, the first bit received. K1[0] is the least significant bit, corresponding to bit 8, the last bit received.

Register 0x0F6: RASE Receive K2

Bit	Type	Function	Default
Bit 7	R	K2[7]	X
Bit 6	R	K2[6]	X
Bit 5	R	K2[5]	X
Bit 4	R	K2[4]	X
Bit 3	R	K2[3]	X
Bit 2	R	K2[2]	X
Bit 1	R	K2[1]	X
Bit 0	R	K2[0]	X

K2[7:0]:

The K2[7:0] bits contain the current K2 code value. The contents of this register are updated when a new K2 code value (different from the current K2 code value) has been received for three consecutive frames. An interrupt may be generated when a new code value is received (using the COAPSE bit in the RASE Interrupt Enable Register). K2[7] is the most significant bit corresponding to bit 1, the first bit received. K2[0] is the least significant bit, corresponding to bit 8, the last bit received.

Register 0x0F7: RASE Receive Z1/S1

Bit	Type	Function	Default
Bit 7	R	Z1/S1[7]	X
Bit 6	R	Z1/S1[6]	X
Bit 5	R	Z1/S1[5]	X
Bit 4	R	Z1/S1[4]	X
Bit 3	R	Z1/S1[3]	X
Bit 2	R	Z1/S1[2]	X
Bit 1	R	Z1/S1[1]	X
Bit 0	R	Z1/S1[0]	X

Z1/S1[3:0]:

The lower nibble of the first Z1/S1 byte contained in the receive stream is extracted into this register. The Z1/S1 byte is used to carry synchronization status messages between line terminating network elements. Z1/S1[3] is the most significant bit corresponding to bit 5, the first bit received. Z1/S1[0] is the least significant bit, corresponding to bit 8, the last bit received. An interrupt may be generated when a byte value is received that differs from the value extracted in the previous frame (using the Z1/S1E bit in the RASE Interrupt Enable Register). In addition, debouncing can be performed where the register is not loaded until eight of the same consecutive nibbles are received. Debouncing is controlled using the Z1/S1_CAP bit in the RASE Configuration/Control register.

Z1/S1[7:4]:

The upper nibble of the first Z1/S1 byte contained in the receive stream is extracted into this register. No interrupt is asserted on the change of this nibble. In addition, when the Z1/S1_CAP bit in the RASE Configuration/Control register selects debouncing, the upper nibble is only updated when eight of the same consecutive lower nibbles are received.

Register 0x0FC: Channel Concatenation Status and Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	AISCV	X
Bit 4	R	LOPCV	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	AISCE	0
Bit 0	R/W	LOPCE	0

LOPCE:

The LOPCE bit is the interrupt enable for the Loss of Pointer Concatenation event. When LOPCE is a logic one, an interrupt is generated when the state of the Loss of Pointer Concatenation indicator changes.

AISCE:

The AISCE bit is the interrupt enable for the Pointer AIS event. When AISCE is a logic one, an interrupt is generated when the state of the Pointer AIS indicator changes.

LOPCV:

The LOPCV bit is the Loss of Pointer Concatenation indicator. When LOPCV is logic one, the STS-3c/STM-1 pointers do not indicate a concatenated payload. When LOPCV and AISCV are both logic zero, a STS-3c/STM-1 payload is indicated.

AISCV:

The ASICV bit is the Pointer AIS indicator. When AISCV is logic one, the STS-3c/STM-1 pointer indicates a pointer AIS condition. When LOPC and AISCV are both logic zero, a STS-3c/STM-1 payload is indicated.

Register 0x0FD: Channel Concatenation Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	AISCI	X
Bit 0	R	LOPCI	X

LOPCI:

A logic one on the LOPCI bit indicates that a transition has occurred on the Loss of Pointer Concatenation indicator. This bit is cleared when this register is read.

AISCI:

A logic one on the AISCI bit indicates that a transition has occurred on the Pointer AIS indicator. This bit is cleared when this register is read.

Register 0x0FE: Channel Serial Interface Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	1
Bit 2	R/W	Reserved	1
Bit 1	R/W	TXDINV	0
Bit 0	R/W	RXDINV	0

RXDINV:

The receive inversion RXDINV controls the polarity of the receive data. When RXDINV is set high, the polarity of the RXD+/- is inverted. When RXDINV is set low, the RXD+/- inputs operate normally.

TXDINV:

The transmit inversion TXDINV controls the polarity of the transmit data. When TXDINV is set high, the polarity of the TXD+/- is inverted. When TXDINV is set low, the TXD+/- outputs operate normally.

Reserved:

The reserved bits must be programmed to their default values for proper operation.

Register 0x0FF: Channel Clock Monitors

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	RCLKA	X
Bit 2	R	TCLKA	X
Bit 1	R	RFCLKA	X
Bit 0	R	TFCLKA	X

This register provides activity monitoring of the channel clocks. When a monitored clock signal makes a low to high transition, the corresponding register bit is set high. The bit will remain high until this register is read, at which point all the bits in this register are cleared. A lack of transitions is indicated by the corresponding register bit reading low. This register should be read at periodic intervals to detect clock failures.

TFCLKA:

The TFCLK active (TFCLKA) bit monitors for low to high transition on the channel's TFCLK internal clock. TFCLKA is set high on a rising edge of Level 2 TFCLK and is set low when this register is read.

RFCLKA:

The RFCLK active (RFCLKA) bit monitors for low to high transition on the channel's RFCLK internal clock. RFCLKA is set high on a rising edge of Level 2 RFCLK and is set low when this register is read.

RCLKA:

The RCLK active (RCLKA) bit monitors for low to high transition on the channel's RCLK receive line rate clock. RCLKA is set high on a rising edge of channel RCLK and is set low when this register is read.

TCLKA:

The TCLK active (TCLKA) bit monitors for low to high transition on the channel's TCLK transmit line rate clock. TCLKA is set high on a rising edge of TCLK and is set low when this register is read.

Register 0x100: S/UNI-1x155 Master Interrupt Status

Bit	Type	Function	Default
Bit 7	R	RDLLI	X
Bit 6		Unused	X
Bit 5	R	TDLLI	X
Bit 4	R	CHNLI	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	STALI	X
Bit 0	R	RAPSI	X

When the interrupt output INTB goes low, this register allows the source of the active interrupt to be identified down to the block level. Further register accesses are required for the block in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

RAPSI:

The RAPSI bit is a logic one when an interrupt request is active from the receive APS interfaces. The APS Interrupt Status and APS FIFO Configuration Status registers must be read in order to determine the block with the active interrupt source.

STALI:

The STALI bit is a logic one when an interrupt request is active from the STAL blocks. Each Channel Cross Connect Control register must be read to identify the channel STALs with the active interrupt source.

CHNLI:

The CHNLI channel interrupt bit is a logic one when an interrupt request is active from the corresponding channel. The channel's Reset/Interrupt Status #1 register or Interrupt Status #2 register must be read in order to determine the block with the active interrupt source.

TDLLI:

The TDLLI bit is a logic one when an interrupt request is active from the TFCLK DLL block. The TFCLK DLL interrupt sources are enabled in the TFCLK DLL Configuration register.

RDLLI:

The RDLLI bit is a logic one when an interrupt request is active from the RFCLK DLL block. The RFCLK DLL interrupt sources are enabled in the RFCLK DLL Configuration register.

Register 0x101: S/UNI-1x155 DCC Interface Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	X
Bit 6	R/W	Reserved	X
Bit 5	R/W	Reserved	X
Bit 4	R/W	Reserved	X
Bit 3	R/W	Reserved	X
Bit 2	R/W	Reserved	X
Bit 1	R/W	Reserved	X
Bit 0	R/W	DCCSEL	0

This register configures the DCC interfaces for section or line DCC operation for the channel.

DCCSEL:

The DCC mode select determines if the DCC interfaces (RDCC and TDCC) are configured for section or line DCC operation. When DCCSEL is high, the associated channel DCC interface is configured for section DCC. When DCCSEL is low, the associated channel DCC interface is configured for line DCC.

Register 0x102: CSPI Clock Synthesis Configuration

Bit	Type	Function	Default
Bit 7	R/W	CSU_RESET	0
Bit 6	R/W	IDDQ_EN	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	CSU_LOCK	X
Bit 2	R/W	MODE[2]	0
Bit 1	R/W	MODE[1]	0
Bit 0	R/W	MODE[0]	0

MODE[2:0]:

The MODE[2:0] selects the mode of the CSU. For proper operation of the S/UNI 1x155, MODE[2:0] should be programmed as “101”.

CSU_LOCK :

The CSU_LOCK bit indicates whether or not the embedded CSU has achieved phase and frequency lock to REFCLK. CSU_LOCK is a logic 1 if the divided down synthesized clock frequency is within 244 ppm of the REFCLK frequency. If REFCLK is removed this bit will indefinitely indicate the status of the CSU prior to disconnecting REFCLK.

IDDQ_EN :

Setting the IDDQ_EN bit to logic 1 forces the embedded CSU into a low power configuration compatible with IDDQ testing. This bit is logically ORed with the IDDQ_EN pin, so a logic 1 on either will force the CSU into low power state.

CSU RESET:

Setting the CSU_RESET bit to logic 1 causes the CSU_RSTB signal passed to the embedded CSU to be held in a low state, and the embedded CSU VCO is reset in the case that it didn’t start up properly.

Register 0x10B: TFCLK DLL Control Status

Bit	Type	Function	Default
Bit 7	R	TFCLKI	X
Bit 6	R	Unused	X
Bit 5	R	ERRORI	X
Bit 4	R	Unused	X
Bit 3		Unused	X
Bit 2	R	ERROR	X
Bit 1	R	Unused	X
Bit 0	R	RUN	X

The DLL Control Status Register provides information of the DLL operation.

RUN:

The DLL lock status register bit RUN indicates the DLL has found an initial lock condition. When the phase detector first indicates lock, RUN is set high. The RUN register bit is cleared only by a system reset or a software reset.

ERROR:

The delay line error register ERROR indicates the DLL is currently at the end of the delay line. ERROR is set high when the DLL tries to move beyond the end of the delay line.

ERRORI:

The error event register bit ERRORI indicates the ERROR register bit has been a logic one. When the ERROR register changes from a logic zero to a logic one, the ERRORI register bit is set to logic one. The ERRORI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

TFCLKI:

The clock event register bit TFCLKI provides a method to monitor activity on the TFCLK clock. When the TFCLK input changes from a logic zero to a logic one, the TFCLKI register bit is set to logic one. The TFCLKI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

Register 0x10C: RFCLK DLL Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	Reserved	0
Bit 3		Unused	X
Bit 2	R/W	ERRORE	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

The DLL Configuration Register controls the basic operation of the DLL for the receive system interface clock RFCLK.

ERRORE:

The DLL error interrupt enable controls the assertion of the INTB output when ERROR is high. When ERRORE is set high, an interrupt is generated upon assertion event of the ERROR register. When ERRORE is set low, changes in the ERROR status do not generate an interrupt.

Register 0x10F: RFCLK DLL Control Status

Bit	Type	Function	Default
Bit 7	R	RFCLKI	X
Bit 6	R	Unused	X
Bit 5	R	ERRORI	X
Bit 4	R	Unused	X
Bit 3		Unused	X
Bit 2	R	ERROR	X
Bit 1	R	Unused	X
Bit 0	R	RUN	X

RUN:

The DLL lock status register bit RUN indicates the DLL has found an initial lock condition. When the phase detector first indicates lock, RUN is set high. The RUN register bit is cleared only by a system reset or a software reset.

ERROR:

The delay line error register ERROR indicates the DLL is currently at the end of the delay line. ERROR is set high when the DLL tries to move beyond the end of the delay line.

ERRORI:

The error event register bit ERRORI indicates the ERROR register bit has been a logic one. When the ERROR register changes from a logic zero to a logic one, the ERRORI register bit is set to logic one. The ERRORI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

RFCLKI:

The clock event register bit RFCLKI provides a method to monitor activity on the RFCLK clock. When the RFCLK input changes from a logic zero to a logic one, the RFCLKI register bit is set to logic one. The RFCLKI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

Register 0x110: APS Configuration and Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	TAPS55	0
Bit 0	R	APSTIP	0

This register controls the APS serial interfaces. Specifically, the RAOP, TAOP and RAPS blocks used for APS functionality.

APSTIP:

The APSTIP bit is set to a logic one when the APS performance monitor registers are being loaded. Writing to the APS Interrupt Status register (0x112) initiates an accumulation interval transfer and loads all the performance monitor registers in the RAOP blocks.

Writing to the S/UNI-1x155 Master Reset and Identity register (0x000) will also cause the APS performance monitor registers to be loaded.

APSTIP remains high while the transfer is in progress, and is set to a logic zero when the transfer is complete. APSTIPO can be polled by a microprocessor to determine when the accumulation interval transfer is complete.

TAPS55:

The force transmit APS (TAPS55) forces the transmit APS serial interfaces to transmit a constant 1/0 pattern. When TAPS55 is set high, the transmit APS serial interfaces are forced to a constant alternating value. When TAPS55 is set low, the transmit APS serial interfaces operated normally.

This feature is used for analog testing of the APS interfaces only.

Register 0x112: APS Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	RAPSI	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	DRCUI	X
Bit 0	R	RAOPI	X

When the interrupt output INTB goes low, this register allows the source of the active interrupt to be identified down to the block level for the APS interfaces. Further register accesses are required for the block in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

RAOPI:

The RSOPI bit is high when an interrupt request is active from the corresponding RAOP block. The RAOP interrupt sources are enabled in each of the RAOP Control/Interrupt Enable Register.

DRCUI:

The DRCUI bit is high when an interrupt request is active from the APS DRCU logic. The APS DRCU interrupt sources are enabled in the APS DRCU Configuration register.

RAPSI:

The RAPSI bit is high when an interrupt request is active from the corresponding RAPS block. The RAPS interrupt sources are enabled in each of the RAPS Configuration Register.

Register 0x113: APS Reset Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Unused	X
Bit 4	R/W	RXAPRST	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Unused	X
Bit 0	R/W	TXAPRST	0

When the interrupt output INTB goes low, this register allows the source of the active interrupt to be identified down to the block level for the APS interface. Further register accesses are required for the block in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

TXAPRST:

The TXAPRST bit allow the transmit APS serial interfaces to be reset under software control. If the TXAPRST bit is a logic one, the transmit APS interface (TAOP and associated logic) is held in reset. This bit is not self-clearing. Therefore, a logic zero must be written to bring the channel out of reset.

Holding the channel in a reset state places it into a low power, stand-by mode. A hardware reset or top level reset using RESET clears the TXAPSRST bit, thus negating the software reset. Otherwise, the effect of the software reset is equivalent to that of a hardware reset.

RXAPRST:

The RXAPRST bits allow the receive APS serial interfaces to be reset under software control. If the RXAPRST bit is a logic one, the receive APS interface (RAOP, RAPS and associated logic) is held in reset. This bit is not self-clearing. Therefore, a logic zero must be written to bring the channel out of reset.

Holding the channel in a reset state places it into a low power, stand-by mode. A hardware reset or top level reset using RESET clears the RXAPSRST bit, thus negating the software reset. Otherwise, the effect of the software reset is equivalent to that of a hardware reset.

Reserved:

These register bits must be set to logic zero for proper operation.

Register 0x114: TAOP Link Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	DS	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	LAIS	0

The Transmit APS Overhead Processor (TAOP) controls the transmit APS interface generating A1/A2 framing and SONET scrambling. One instance of this block is used for the APS link.

LAIS:

The LAIS bit controls the insertion of line alarm indication signal (AIS). When LAIS is set to logic one, the TSOP inserts AIS into the transmit SONET/SDH stream. Activation or deactivation of line AIS insertion is synchronized to frame boundaries. Line AIS insertion results in all bits of the SONET/SDH frame being set to 1 prior to scrambling except for the section overhead.

DS:

The DS bit is set to logic one to disable the scrambling of the STS-3c/STM-1 stream. When DS is a logic zero, scrambling is enabled.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x115: TAOP Link Diagnostic

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	DLOS	0
Bit 1	R/W	DBIP8	0
Bit 0	R/W	DFP	0

The Transmit APS Overhead Processor (TAOP) controls the transmit APS interface generating A1/A2 framing and SONET scrambling. One instance of this block is used for the APS link.

DFP:

The DFP bit controls the insertion of a single bit error continuously in the most significant bit (bit 1) of the A1 section overhead framing byte. When DFP is set to logic one, the A1 bytes are set to 0x76 instead of 0xF6.

DBIP8:

The DBIP8 bit controls the insertion of bit errors continuously in the section BIP-8 byte (B1). When DBIP8 is set to logic one, the B1 byte is inverted.

DLOS:

The DLOS bit controls the insertion of all zeros in the STS-3c/STM-1 stream. When DLOS is set to logic one, the transmit stream is forced to 0x00.

Register 0x118: RAOP Link Control/Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	BLKBIP	0
Bit 6	R/W	DDS	0
Bit 5	W	FOOF	X
Bit 4	R/W	ALGO2	0
Bit 3	R/W	BIPEE	0
Bit 2	R/W	LOSE	0
Bit 1	R/W	LOFE	0
Bit 0	R/W	OOFE	0

The Receive APS Overhead Processor (RAOP) controls the receive APS interface SONET framing and descrambling as well as performance monitoring the APS link. One instance of this block is used for the APS link.

OOFE:

The OOFE bit is an interrupt enable for the out-of-frame alarm. When OOFE is set to logic one, an interrupt is generated when the out-of-frame alarm changes state.

LOFE:

The LOFE bit is an interrupt enable for the loss of frame alarm. When LOFE is set to logic one, an interrupt is generated when the loss of frame alarm changes state.

LOSE:

The LOSE bit is an interrupt enable for the loss of signal alarm. When LOSE is set to logic one, an interrupt is generated when the loss of signal alarm changes state.

BIPEE:

The BIPEE bit is an interrupt enable for the section BIP-8 errors. When BIPEE is set to logic one, an interrupt is generated when a section BIP-8 error (B1) is detected.

ALGO2:

The ALGO2 bit position selects the framing algorithm used to determine and maintain the frame alignment. When a logic one is written to the ALGO2 bit position, the framer is enabled to use the second of the framing algorithms where only the first A1 framing byte and the first 4 bits of the last A2 framing byte (12 bits total) are examined. This algorithm examines only 12 bits of the framing pattern regardless; all other framing bits are ignored. When a logic zero is written to the ALGO2 bit position, the framer is enabled to use the first of the framing algorithms where all the A1 framing bytes and all the A2 framing bytes are examined.

FOOF:

The FOOF bit controls the framing of the RAOP. When a logic one is written to FOOF, the RAOP is forced out of frame at the next frame boundary. The FOOF bit is a write only bit. Register reads may yield a logic one or a logic zero.

DDS:

The DDS bit is set to logic one to disable the descrambling of the APS stream. When DDS is a logic zero, descrambling is enabled.

BLKBIP:

The BLKBIP bit position enables the accumulating of section BIP word errors. When a logic one is written to the BLKBIP bit position, one or more errors in the BIP-8 byte result in a single error being accumulated in the B1 error counter. When a logic zero is written to the BLKBIP bit position, all errors in the B1 byte are accumulated in the B1 error counter.

Register 0x119: RAOP Link Status/Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	BIPEI	X
Bit 5	R	LOSI	X
Bit 4	R	LOFI	X
Bit 3	R	OOFI	X
Bit 2	R	LOSV	X
Bit 1	R	LOFV	X
Bit 0	R	OOFV	X

The Receive APS Overhead Processor (RAOP) controls the receive APS interface SONET framing and descrambling as well as performance monitoring the APS link. One instance of this block is used for the APS link.

OOFV:

The OOFV bit is read to determine the out-of-frame state of the RSOP. When OOFV is high, the RAOP is out of frame. When OOFV is low, the RSOP is in-frame.

LOFV:

The LOFV bit is read to determine the loss of frame state of the RSOP. When LOFV is high, the RAOP has declared loss of frame.

LOSV:

The LOSV bit is read to determine the loss of signal state of the RSOP. When LOSV is high, the RAOP has declared loss of signal.

OOFI:

The OOFI bit is the out-of-frame interrupt status bit. OOFI is set high when a change in the out-of-frame state occurs. This bit is cleared when this register is read.

LOFI:

The LOFI bit is the loss of frame interrupt status bit. LOFI is set high when a change in the loss of frame state occurs. This bit is cleared when this register is read.

LOSI:

The LOSI bit is the loss of signal interrupt status bit. LOSI is set high when a change in the loss of signal state occurs. This bit is cleared when this register is read.

BIPEI:

The BIPEI bit is the section BIP-8 interrupt status bit. BIPEI is set high when a section layer (B1) bit error is detected. This bit is cleared when this register is read.

Register 0x11A: RAOP Link Section BIP-8 LSB

Bit	Type	Function	Default
Bit 7	R	SBE[7]	X
Bit 6	R	SBE[6]	X
Bit 5	R	SBE[5]	X
Bit 4	R	SBE[4]	X
Bit 3	R	SBE[3]	X
Bit 2	R	SBE[2]	X
Bit 1	R	SBE[1]	X
Bit 0	R	SBE[0]	X

Register 0x11B: RAOP Link Section BIP-8 MSB

Bit	Type	Function	Default
Bit 7	R	SBE[15]	X
Bit 6	R	SBE[14]	X
Bit 5	R	SBE[13]	X
Bit 4	R	SBE[12]	X
Bit 3	R	SBE[11]	X
Bit 2	R	SBE[10]	X
Bit 1	R	SBE[9]	X
Bit 0	R	SBE[8]	X

The Receive APS Overhead Processor (RAOP) controls the receive APS interface SONET framing and descrambling as well as performance monitoring the APS link. One instance of this block is used for the APS link.

SBE[15:0]:

Bits SBE[15:0] represent the number of section BIP-8 errors (individual or block) that have been detected since the last time the error count was polled. The error count is polled by writing to either of the RAOP Section BIP-8 Register addresses. Such a write transfers the internally accumulated error count to the Section BIP-8 registers within approximately 7 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that ensures that coincident events are not lost.

The count can also be polled by writing to the S/UNI-1x155 Master Reset and Identity register (0x000). Writing to register address 0x000 loads all counter registers in the channel and APS link.

The count can also be polled by writing to the APS Interrupt Status register (0x112). Writing to register address 0x11A loads all counter registers in the RAOP blocks.

Register 0x11C: RAPS Link Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	SENB	0
Bit 4	R/W	Reserved	0
Bit 3		Unused	X
Bit 2	R	LOTI	X
Bit 1		Unused	X
Bit 0	R	DOOLI	X

The Receive APS Interface (RAPS) controls the receive APS interface SONET framing. One instance of this block is used for the APS link.

DOOLI:

The DOOLI bit is the data out of lock interrupt status bit. DOOLI is set high when the DOOLV bit changes state, indicating that either the DCRU has locked to the incoming data stream or has gone out of lock. DOOLI is cleared when this register is read.

LOTI:

The LOTI bit is the loss of transition interrupt status bit. LOTI is set high when a loss of transition event occurs. A loss of transition is defined as more than 96 consecutive ones or zeros received. LOTI is cleared when this register is read.

SENB:

The loss of signal transition detector enable (SENB) bit enables the declaration of loss of transition (LOT) when more than 96 consecutive ones or zeros occurs in the receive data. When SENB is a logic zero, a loss of transition is declared when more than 96 consecutive ones or zeros occurs in the receive data. When SENB is a logic one, a loss of transition is never declared.

Reserved:

These registers must be programmed to logic zero for proper operation.

Register 0x11D: RAPS Link Status

Bit	Type	Function	Default
Bit 7	R	Reserved	X
Bit 6	R	LOTV	X
Bit 5	R	ROOLV	X
Bit 4	R	DOOLV	X
Bit 3		Unused	X
Bit 2	R/W	LOTE	0
Bit 1	R/W	ROOLE	0
Bit 0	R/W	DOOLE	0

The Receive APS Interface (RAPS) controls the receive APS interface SONET framing. One instance of this block is used for the APS link.

DOOLE:

The DOOLE bit is an interrupt enable for the recovered data out of lock status. When DOOLE is set to logic one, an interrupt is generated upon assertion and negation events of the DOOLV register. When ROOLE is set low, changes in the DOOL status do not generate an interrupt.

ROOLE:

The ROOLE bit enables the reference out of lock indication interrupt. When ROOLE is set high, an interrupt is generated upon assertion and negation events of the ROOLV register. When ROOLE is set low, changes in the ROOL status do not generate an interrupt.

LOTE:

The LOTE bit enables the loss of transition indication interrupt. When LOTE is set high, an interrupt is generated upon assertion events of the LOTV register. When LOTE is set low, changes in the LOTV status do not generate an interrupt.

DOOLV:

The recovered data out of lock status indicates the clock recovery phase locked loop is unable to recover and lock to the input data stream. DOOLV is a logic one if the recovered APS serial stream is not within approximately 488ppm of the REFCLK frequency of if no transitions have occurred on the APS link for more than 96 bits.

ROOLV:

The recovered reference out of lock status indicates the clock recovery phase locked loop is unable to lock to the reference clock on REFCLK. ROOLV is a logic one if the recovered APS serial stream is not within approximately 488ppm of the REFCLK frequency. At startup, ROOLV may remain high for several hundred millisecond while the DRU obtains lock.

LOTV:

The loss of transition status indicates that at least 97 consecutive ones or zeros have been received. LOTV is a logic zero if fewer than 97 consecutive ones or zeros have been received. LOTV is a logic one if more than 96 consecutive ones or zeros have been received.

Register 0x120: DRU Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	RUN	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R/W	Reserved	0

RUN:

The DLL lock status register bit RUN indicates the DRU has found an initial delay line lock. When the DRU is attempting to recover the incoming serial stream, RUN is set high. The RUN register bit is cleared only by a system reset or a software reset.

Reserved:

All reserved bits must be programmed to zero for proper operation.

Register 0x130: Level 2 Receive Address

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	RADR[4]	0
Bit 3	R/W	RADR[3]	0
Bit 2	R/W	RADR[2]	0
Bit 1	R/W	RADR[1]	0
Bit 0	R/W	RADR[0]	0

The Level 2 Receive Address registers controls the UTOPIA/POS-PHY Level 2 device address on the receive direction.

RADR[4:0]:

The receive UTOPIA/POS-PHY Level 2 interface address specifies the Level 2 address required on the TRDR[4:0] pins to select the S/UNI-1x155 when RENB transitions low.

Register 0x131: Level 2 Transmit Address

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	TADR[4]	0
Bit 3	R/W	TADR[3]	0
Bit 2	R/W	TADR[2]	0
Bit 1	R/W	TADR[1]	0
Bit 0	R/W	TADR[0]	0

The Level 2 Transmit Address registers controls the UTOPIA/POS-PHY Level 2 device address on the transmit direction.

TADR[4:0]:

The transmit UTOPIA/POS-PHY Level 2 interface address specifies the Level 2 address required on the TADR[4:0] pins to select the S/UNI-1x155 when TENB transitions low.

Register 0x132: Channel Receive Connect Select

Bit	Type	Function	Default
Bit 7	R/W	RXEN	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	RSEL	0

The Receive Connect Select registers controls the source of receive path.

RSEL:

The receive cross connect select (RSEL) determines the source of receive path for the channel. When RXEN is low, RSEL is ignored. When RXEN is high, RSEL specifies the source channel for the Receive Path Processor (RPOP) of the channel. See Table 19 1+1 APS Configuration for more information.

RXEN:

The receive cross connect enable (RXEN) controls when the channel's Receive Path Processor (RPOP) can cross connect with the APS channel. When RXEN is low, the channel operates normally. When RXEN is high, the APS channel is enabled. RXEN also multiplexes the alarm signal.

Register 0x133: Channel Transmit Connect Select

Bit	Type	Function	Default
Bit 7	R/W	TXEN	0
Bit 6	R/W	PROCM	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	TSEL	0

The Transmit Connect Select registers control the source of transmit path.

TSEL:

The transmit cross connect select (TSEL) determines the source of transmit path for the channel. When TXEN is low, the TSEL is ignored. When TXEN is high, TSEL specifies the source channel for the Transmit Path Processor (TPOP) of the channel. See Table 19 1+1 APS Configuration for more information.

PROCM:

The transmit APS protection mode select (PROCM) configures the channel for protection or working operation. When PROCM is set low, the channel's receive path is sent over the transmit APS link (channel is operating as a protection link). When PROCM is set high, the channel's transmit path is set over the transmit APS link (channel path is being bridged to another channel).

TXEN:

The transmit cross connect enable (TXEN) controls when a channel's Transmit Path Processor (TPOP) can cross connect with the APS channel. When TXEN is low, the channel operates normally. When TXEN is high, the channel cross connect is enabled.

Register 0x134: Channel Connect Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	CSTALI	X
Bit 2	R	Reserved	X
Bit 1	R/W	CHFRST	0
Bit 0	R/W	TAPSRST	0

The Connect Control registers provides configuration and status .

TAPSRST:

The transmit APS reset (TAPSRST) bit allows the STAL blocks associated with the channel to be reset under software control. If the TAPSRST bit is a logic one, the STAL blocks for the channel are held in reset. This bit is not self-clearing. Therefore, a logic zero must be written to bring the APS logic out of reset.

Holding the STAL blocks in a reset state places it into a low power, stand-by mode. A hardware reset or top level reset using RESET clears the TAPSRST bit, thus negating the software reset. Otherwise, the effect of the channel software reset is equivalent to that of a hardware reset.

CHFRST:

The transmit channel FIFO reset register (CHFRST) is used to reset the 8-byte transmit cross connect FIFO. When the CHFRST bit is set high, the channel's transmit connect FIFO is held in reset. The FIFO is held in reset until the CHFRST is set low.

When the FIFO is reset, the FIFO is initialized such that the FIFO is centered (that is, the fill level of the FIFO is 4 bytes).

CSTALI:

The CSTALI bit is a logic one when an interrupt request is active from the channel STAL blocks. The STAL Control and Interrupt Status registers for the STAL associated with the channel must be read in order to identify the STAL with the active interrupt request.

Register 0x138: STAL Channel Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	H4BYP	0
Bit 5	R/W	Reserved	0
Bit 4		Unused	X
Bit 3	R/W	Reserved	0
Bit 2	R/W	ESEE	0
Bit 1	R/W	OPJEE	0
Bit 0	R/W	IPAIS	0

These STAL blocks perform the pointer processing required for the transmit APS interface. The other STAL blocks are slaved to these STAL blocks.

IPAIS:

The insert path AIS bits control the insertion of Path AIS in the transmit APS stream. When IPAIS is set high, path AIS is inserted in the outgoing bus. The pointer bytes (H1, H2, and H3) and the entire synchronous payload envelope (virtual container) is set to all ones. Normal operation resumes when the IPAIS bit is set low.

OPJEE:

The transmit APS stream pointer justification event interrupt enable bit (OPJEE) controls the activation of the interrupt output when a pointer justification is inserted in the APS stream. When OPJEE is set high, insertion of pointer justification events in the transmit APS stream will assert the INTB output. When OPJEE is set low, insertion of pointer justification events will not affect INTB.

ESEE:

The elastic store error interrupt enable bit (ESEE) controls the assertion of INTB when a FIFO underflow or overflow has been detected in the elastic store. When ESEE is set high, FIFO flow error events will assert the INTB output. When ESEE is set low, FIFO flow error events will not affect INTB.

H4BYP:

The tributary multiframe bypass bit (H4BYP) controls whether the H4 byte in the path overhead is over-written by an internally generated sequence. When H4BYP is set high, the H4 byte carried in the incoming stream is placed in the outgoing stream unchanged. When H4BYP is set low, the H4 byte is replaced by the sequence 'hFC, 'hFD, 'hFE and 'hFF. The phase of the four frames in the multiframe is synchronized by the IV1 pulse.

Reserved:

These register bits must be set to logic zero for proper operation.

Register 0x139: STAL Channel Control and Interrupt Status

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	1
Bit 4	R/W	Reserved	0
Bit 3	R	ESEI	X
Bit 2	R	PPJI	X
Bit 1	R	NPJI	X
Bit 0	R/W	DLOP	0

These STAL blocks perform the pointer processing required for the transmit APS interface. The other STAL blocks are slaved to these STAL blocks.

DLOP:

The diagnose loss of pointer control bit (DLOP) allows downstream pointer processing elements to be diagnosed. When DLOP is set high, the new data flag (NDF) field of the payload pointer inserted in the APS stream is inverted causing downstream pointer processing elements to enter a loss of pointer (LOP) state.

NPJI:

The transmit APS stream negative pointer justification interrupt status bit (NPJI) is set high when the STAL inserts a negative pointer justification event on the APS stream.

PPJI:

The transmit APS stream positive pointer justification interrupt status bit (PPJI) is set high when the STAL inserts a positive pointer justification event on the APS stream.

ESEI:

The elastic store error interrupt status bit (ESEI) is set high when STAL detects a FIFO underflow or overflow event.

Register 0x13A: STAL Channel Alarm and Diagnostic Control

Bit	Type	Function	Default
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	ESAIS	0
Bit 0	R/W	Reserved	0

These STAL blocks perform the pointer processing required for the transmit APS interface. The other STAL blocks are slaved to these STAL blocks.

ESAIS:

The elastic store error path AIS insertion enable bit (ESAIS) controls the insertion of path AIS in the transmit APS stream when a FIFO underflow or overflow has been detected in the elastic store. When ESAIS is set high, detection of FIFO flow errors will cause path AIS to be inserted in the outgoing stream for at least three frames. When ESAIS is set low, path AIS is not inserted as a result of FIFO errors.

Reserved:

All reserved bits must be programmed to zero for proper operation.

Register 0x13C, 0x140: STAL Channel Slave #0, #1 Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4		Unused	X
Bit 3	R/W	Reserved	0
Bit 2	R/W	ESEE	0
Bit 1	R/W	OPJEE	0
Bit 0	R/W	IPAIS	0

These STAL blocks perform the pointer processing required for the transmit APS interface. The other STAL blocks are slaved to these STAL blocks.

IPAIS:

The insert path AIS bits control the insertion of Path AIS in the transmit APS stream. When IPAIS is set high, path AIS is inserted in the outgoing bus. The pointer bytes (H1, H2, and H3) and the entire synchronous payload envelope (virtual container) is set to all ones. Normal operation resumes when the IPAIS bit is set low.

OPJEE:

The transmit APS stream pointer justification event interrupt enable bit (OPJEE) controls the activation of the interrupt output when a pointer justification is inserted in the APS stream. When OPJEE is set high, insertion of pointer justification events in the transmit APS stream will assert the INTB output. When OPJEE is set low, insertion of pointer justification events will not affect INTB.

ESEE:

The elastic store error interrupt enable bit (ESEE) controls the assertion of INTB when a FIFO underflow or overflow has been detected in the elastic store. When ESEE is set high, FIFO flow error events will assert the INTB output. When ESEE is set low, FIFO flow error events will not affect INTB.

Reserved:

These register bits must be set to logic zero for proper operation.

Register 0x13D, 0x141: STAL Channel Slave #0, #1 Control and Interrupt Status

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	1
Bit 4	R/W	Reserved	0
Bit 3	R	ESEI	X
Bit 2	R	PPJI	X
Bit 1	R	NPJI	X
Bit 0	R/W	DLOP	0

These STAL blocks perform the pointer processing required for the transmit APS interface. The other STAL blocks are slaved to these STAL blocks.

DLOP:

The diagnose loss of pointer control bit (DLOP) allows downstream pointer processing elements to be diagnosed. When DLOP is set high, the new data flag (NDF) field of the payload pointer inserted in the APS stream is inverted causing downstream pointer processing elements to enter a loss of pointer (LOP) state.

NPJI:

The transmit APS stream negative pointer justification interrupt status bit (NPJI) is set high when the STAL inserts a negative pointer justification event on the APS stream.

PPJI:

The transmit APS stream positive pointer justification interrupt status bit (PPJI) is set high when the STAL inserts a positive pointer justification event on the APS stream.

ESEI:

The elastic store error interrupt status bit (ESEI) is set high when STAL detects a FIFO underflow or overflow event.

Register 0x13E, 0x142: STAL Channel #0 Slave #0, #1 Alarm and Diagnostic Control

Bit	Type	Function	Default
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	ESAIS	0
Bit 0	R/W	Reserved	0

These STAL blocks perform the pointer processing required for the transmit APS interface. The other STAL blocks are slaved to these STAL blocks.

ESAIS:

The elastic store error path AIS insertion enable bit (ESAIS) controls the insertion of path AIS in the transmit APS stream when a FIFO underflow or overflow has been detected in the elastic store. When ESAIS is set high, detection of FIFO flow errors will cause path AIS to be inserted in the outgoing stream for at least three frames. When ESAIS is set low, path AIS is not inserted as a result of FIFO errors.

Reserved:

All reserved bits must be programmed to zero for proper operation.

12 Test Features Description

Simultaneously asserting (low) the CSB, RDB and WRB inputs causes all digital output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the S/UNI-1x155. Test mode registers (as opposed to normal mode registers) are selected when TRS (A[9]) is high.

In addition, the S/UNI-1x155 also supports a standard IEEE 1149.1 five-signal JTAG boundary scan test port for use in board testing. All digital device inputs may be read and all digital device outputs may be forced via the JTAG test port.

Table 12 Test Mode Register Memory Map

Address	Register
0x000-0x1FF	Normal Mode Registers
0x200	Master Test Register
0x201-0x3FF	Reserved For Production Test

12.1 Master Test and Test Configuration Registers

Notes on Test Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence, unused register bits should be masked off by software when read.

2. Writeable test mode register bits are not initialized upon reset unless otherwise noted.

Register 0x200: Master Test Register

Bit	Type	Function	Default
Bit 7	R/W	BYPASS	0
Bit 6		Unused	X
Bit 5	W	PMCATST	X
Bit 4	W	PMCTST	X
Bit 3	W	DBCTRL	X
Bit 2	R/W	Reserved	0
Bit 1	W	HIZDATA	X
Bit 0	R/W	HIZIO	0

This register is used to enable S/UNI-1x155 test features. All bits, except PMCTST, PMCATST and BYPASS are reset to zero by a reset of the S/UNI-1x155 using either the RSTB input or the Master Reset register. PMCTST are reset when CSB is high. PMCTST and PMCATST can also be reset by writing a logic zero to the corresponding register bit.

HIZIO, HIZDATA:

The HIZIO and HIZDATA bits control the tri-state modes of the S/UNI-1x155. While the HIZIO bit is a logic one, all output pins of the S/UNI-1x155 except the data bus and output TDO are held tri-state. The microprocessor interface is still active. While the HIZDATA bit is a logic one, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles. The HIZDATA bit is overridden by the DBCTRL bit.

DBCTRL:

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic one and PMCTST is set to logic one, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin high causes the S/UNI-1x155 to drive the data bus and holding the CSB pin low tri-states the data bus. The DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit is used to measure the drive capability of the data bus driver pads.

PMCTST:

The PMCTST bit is used to configure the S/UNI-1x155 for PMC's manufacturing tests. When PMCTST is set to logic one, the S/UNI-1x155 microprocessor port becomes the test access port used to run the PMC "canned" manufacturing test vectors. The PMCTST bit can be cleared by setting CSB to logic one and RSTB to logic zero or by writing logic zero to the bit.

PMCATST:

The PMCATST bit is used to configure the analog portion of the S/UNI-1x155 for PMC's manufacturing tests. The PMCTST bit can be cleared by setting CSB to logic one and RSTB to logic zero or by writing logic zero to the bit.

BYPASS:

The BYPASS bit forces the reference clock (REFCLK) to directly clock the channel's parallel-to-serial converter to generate the serial transmit stream (TXD+/-). BYPASS is available for PMC manufacturing test purposes only.

The CSU is not held in reset when BYPASS is high. The CSU may be held in reset by asserting the CSURESET register in the CSPI block.

Reserved:

The reserved bit must be programmed to logic zero for proper operation.

12.2 JTAG Test Port

The JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more details on the JTAG port, please refer to the Operation section.

Table 13 Instruction Register (Length - 3 bits)

Instructions	Selected Register	Instruction Codes, IR[2:0]
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

Table 14 S/UNI-1x155 Identification Register

Length	32 bits
Version Number	0x0
Part Number	0x5384
Manufacturer's Identification Code	0x0CD
Device Identification	0x053840CD

Table 15 S/UNI-1x155 Boundary Scan Register

Pin/Enable	Register Bit	Cell Type	Device I.D.
TDAT[4]	129	IN_CELL	0
TDAT[6]	128	IN_CELL	0
TDAT[5]	127	IN_CELL	0
TDAT[9]	126	IN_CELL	0
TDAT[8]	125	IN_CELL	0
TDAT[7]	124	IN_CELL	1
TDAT[11]	123	IN_CELL	0
TDAT[10]	122	IN_CELL	1
TPRTY	121	IN_CELL	0
TDAT[15]	120	IN_CELL	0
TDAT[12]	119	IN_CELL	1
TDAT[14]	118	IN_CELL	1
TDAT[13]	117	IN_CELL	1

Pin/Enable	Register Bit	Cell Type	Device I.D.
D[4]	116	IO_CELL	0
D_4_EN	115	OUT_CELL	0
TSEN	114	IN_CELL	0
A[1]	113	IN_CELL	0
A[0]	112	IN_CELL	1
A[3]	111	IN_CELL	0
A[2]	110	IN_CELL	0
A[4]	109	IN_CELL	0
A[8]	108	IN_CELL	0
A[5]	107	IN_CELL	0
A[7]	106	IN_CELL	0
A[6]	105	IN_CELL	1
A[9]	104	IN_CELL	1
INTB	103	OUT_CELL	0
INT_EN	102	OUT_CELL	0
RDB	101	IN_CELL	1
CSB	100	IN_CELL	1
RSTB	99	IN_CELL	0
WRB	98	IN_CELL	1
ALE	97	IN_CELL	-
D[2]	96	IO_CELL	-
D_2_EN	95	OUT_CELL	-
D[1]	94	IO_CELL	-
D_1_EN	93	OUT_CELL	-
D[0]	92	IO_CELL	-
D_0_EN	91	OUT_CELL	-
D[7]	90	IO_CELL	-
D_7_EN	89	OUT_CELL	-
D[3]	88	IO_CELL	-
D_3_EN	87	OUT_CELL	-
D[5]	86	IO_CELL	-
D_5_EN	85	OUT_CELL	-
D[6]	84	IO_CELL	-
D_6_EN	83	OUT_CELL	-
SDTTL	82	IN_CELL	-
APECLV	81	IN_CELL	-
SPECLV	80	IN_CELL	-
REFCLK	79	IN_CELL	-
RALRM	78	OUT_CELL	-
TDCC	77	IN_CELL	-

Pin/Enable	Register Bit	Cell Type	Device I.D.
TDCLK	76	OUT_CELL	-
RDCLK	75	OUT_CELL	-
RDCC	74	OUT_CELL	-
RPOHFP	73	OUT_CELL	-
RPOHCLK	72	OUT_CELL	-
RPOH	71	OUT_CELL	-
TPOH	70	IN_CELL	
RTOHFP	69	OUT_CELL	-
TPOHEN	68	IN_CELL	-
RTOHCLK	67	OUT_CELL	-
TPOHFP	66	OUT_CELL	-
TPOHCLK	65	OUT_CELL	-
RTOH	64	OUT_CELL	-
TTOHCLK	63	OUT_CELL	-
TTOHFP	62	OUT_CELL	-
TFPI	61	IN_CELL	-
POS_ATMB	60	IN_CELL	-
TTOHEN	59	IN_CELL	-
TCLK	58	OUT_CELL	-
TTOH	57	IN_CELL	-
ROEB	56	OUT_CELL	-
RDAT[1]	55	OUT_CELL	-
RDAT[2]	54	OUT_CELL	-
RCLK	53	OUT_CELL	-
RDAT[0]	52	OUT_CELL	-
RFPO	51	OUT_CELL	-
TFPO	50	OUT_CELL	-
RDAT[5]	49	OUT_CELL	-
RDAT[3]	48	OUT_CELL	-
RDAT[4]	47	OUT_CELL	-
RDAT[6]	46	OUT_CELL	-
RDAT[8]	45	OUT_CELL	-
RDAT[7]	44	OUT_CELL	-
RDAT[9]	43	OUT_CELL	-
RDAT[10]	42	OUT_CELL	-
RDAT[11]	41	OUT_CELL	-
TCA_PTPA_EN	40	OUT_CELL	-
STPA_EN	39	OUT_CELL	-
RCA_RPA_EN	38	OUT_CELL	-
RDAT[13]	37	OUT_CELL	-

Pin/Enable	Register Bit	Cell Type	Device I.D.
RDAT[12]	36	OUT_CELL	-
RDAT[15]	35	OUT_CELL	-
RDAT[14]	34	OUT_CELL	-
RVAL	33	OUT_CELL	-
RCA_RPA	32	OUT_CELL	-
RMOD	31	OUT_CELL	-
RSOC_RSOP	30	OUT_CELL	-
RPRTY	29	OUT_CELL	-
RENB	28	IN_CELL	-
REOP	27	OUT_CELL	-
RERR	26	OUT_CELL	-
RADR[4]	25	IN_CELL	-
RADR[3]	24	IN_CELL	-
RADR[2]	23	IN_CELL	-
XOFF	22	IN_CELL	-
RADR[1]	21	IN_CELL	-
RFCLK	20	IN_CELL	-
RADR[0]	19	IN_CELL	-
TADR[3]	18	IN_CELL	-
TADR[4]	17	IN_CELL	-
TFCLK	16	IN_CELL	-
TADR[2]	15	IN_CELL	-
TCA_PTPA	14	OUT_CELL	-
TSOC_TSOP	13	IN_CELL	-
STPA	12	OUT_CELL	-
TADR[0]	11	IN_CELL	-
TADR[1]	10	IN_CELL	-
TEOP	9	IN_CELL	-
TMOD	8	IN_CELL	-
TDAT[0]	7	IN_CELL	-
TDAT[1]	6	IN_CELL	-
TENB	5	IN_CELL	-
TERR	4	IN_CELL	-
TDAT[3]	3	IN_CELL	-
TDAT[2]	2	IN_CELL	-
HIZ	1	OUT_CELL	-
TCK		TAP Input	-
TMS		TAP Input	-
TDI		TAP Input	-
TDO		TAP Output	-

Pin/Enable	Register Bit	Cell Type	Device I.D.
TRSTB		TAP Input	-

Notes:

1. Enable "pinname_EN" tri-states pin "pinname" when set high. ROEB tri states the UL2/PL2 receive signals
2. HIZ is the active low output enable for all OUT_CELL types except D[7:0] and INTB.
3. TDAT[4] is the first bit of the boundary scan chain closest to the TDI TAP input.

12.2.1 Boundary Scan Cells

In the following diagrams, CLOCK-DR is equal to TCK when the current controller state is SHIFT-DR or CAPTURE-DR, and unchanging otherwise. The multiplexer in the center of the diagram selects one of four inputs, depending on the status of select lines G1 and G2. The ID Code bit is as listed in the Boundary Scan Register table located above.

Figure 11 Input Observation Cell (IN_CELL)

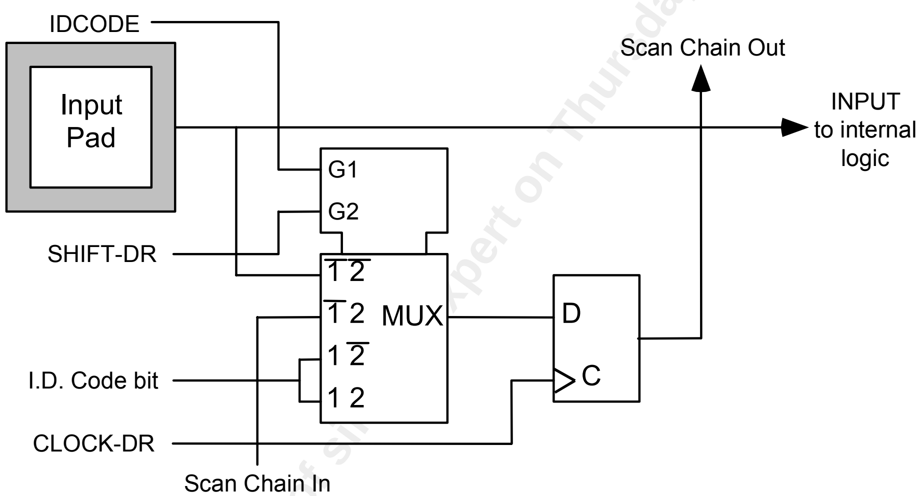


Figure 12 Output Cell (OUT_CELL)

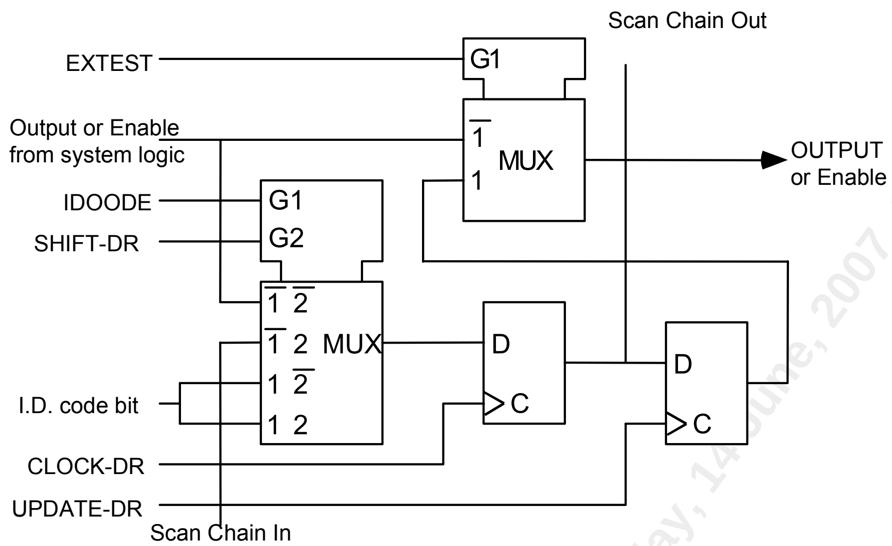


Figure 13 Bi-directional Cell (IO_CELL)

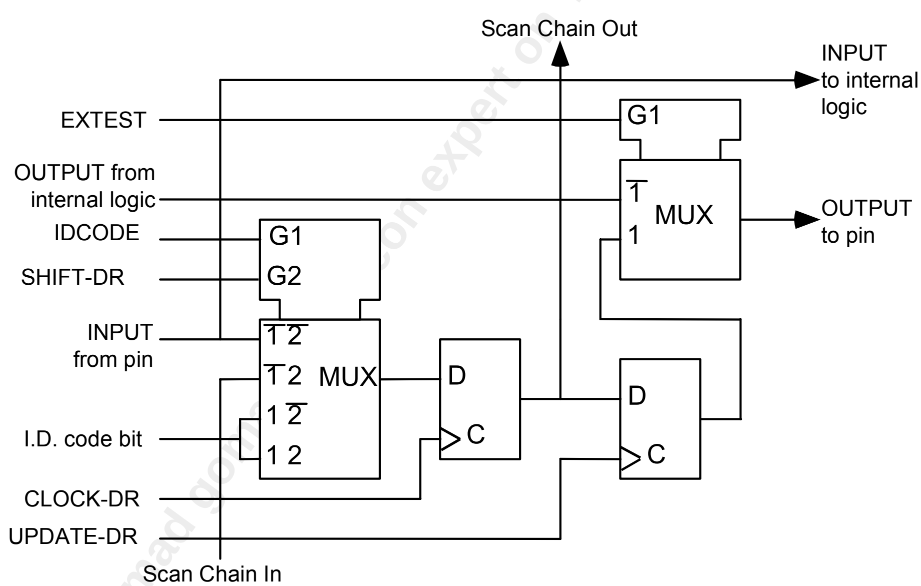
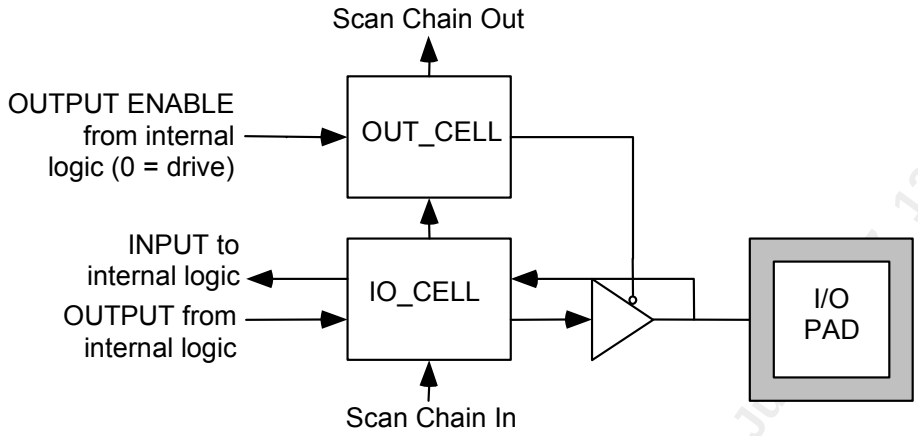


Figure 14 Layout of Output Enable and Bidirectional Cells



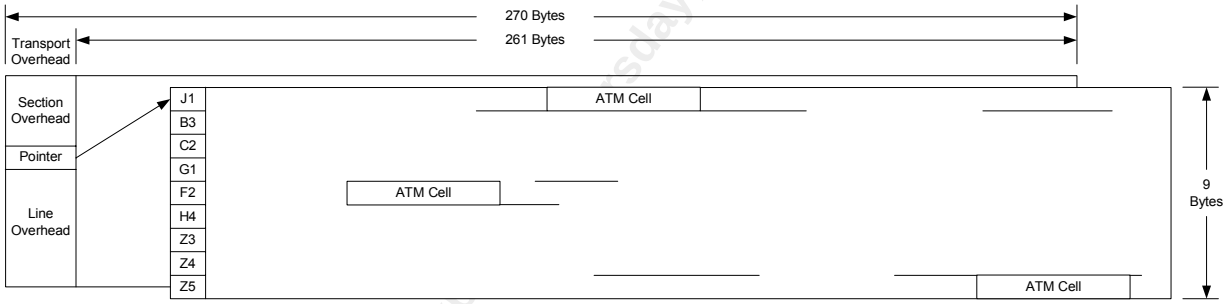
13 Operation

13.1 SONET/SDH Frame Mappings and Overhead Byte Usage

13.1.1 ATM Mapping

The S/UNI-1x155 processes the ATM cell mapping for STS-3c/STM-1 as shown below in Figure 15. The S/UNI-1x155 processes the transport and path overhead required to support ATM UNIs and NNIs. In addition, the S/UNI-1x155 provides support for the APS bytes, the data communication channels and provides full control and observability of the transport and path overhead bytes through register access. In Figure 15, the STS-3c/STM-1 mapping is shown. In this mapping, three stuff columns are included in the SPE. No other options are provided.

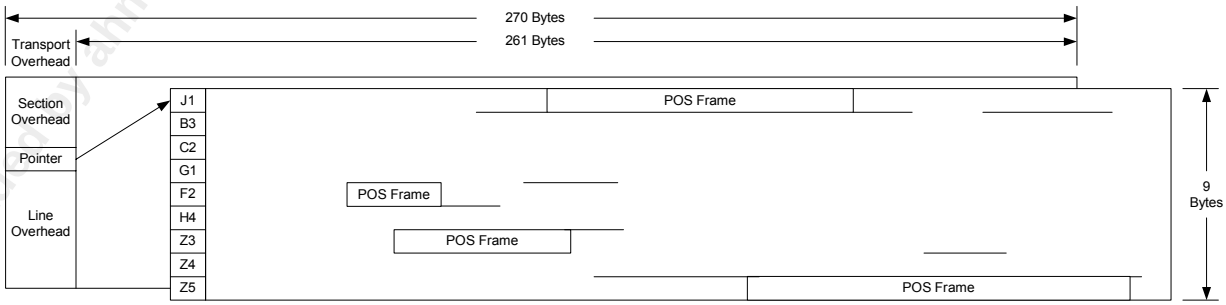
Figure 15 ATM Mapping into the STS-3c/STM-1 SPE



13.1.2 Packet over SONET/SDH Mapping

The S/UNI-1x155 processes the Packet over SONET/SDH mapping for STS-3c/STM-1 as shown below in Figure 16. The S/UNI-1x155 processes the transport and path overhead required to support Packet over SONET/SDH applications. In addition, the S/UNI-1x155 provides support for the APS bytes, the data communication channels and provides full control and observability of the transport and path overhead bytes through register access. In Figure 16, the STS-3c/STM-1 mapping is shown. In this mapping, the entire SPE is used for POS Frames.

Figure 16 POS Mapping into the STS-3c/STM-1 SPE



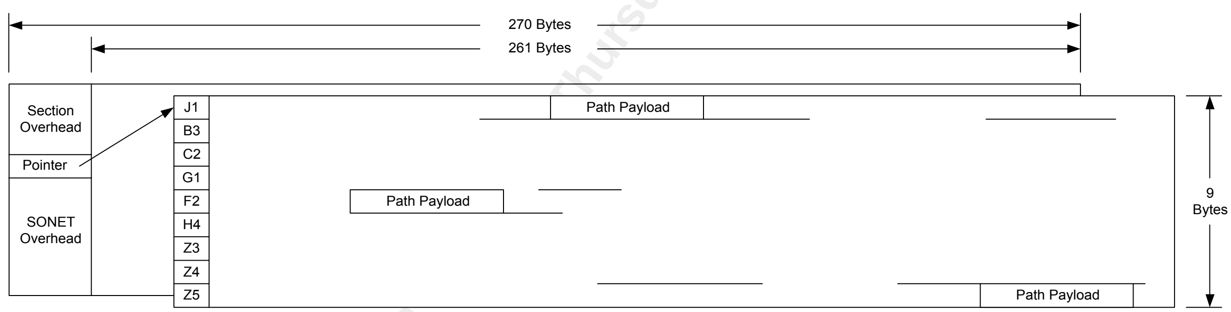
13.1.3 APS Interface Mapping

The APS serial interface is used to pass SONET/SDH STS-3c/STM-1 path information between two S/UNI-1x155 devices using one 155.52 Mbit/s STS-12/STM-4 interface. The APS interface passes the path overhead and payload of one channel transparently over the link. The section overhead contains valid A1, A2, B1, D1, D2 and D3 bytes. The Line overhead is invalid. Figure 17 shows the mapping.

When the APS interface is carrying a transmit path being bridged, the pointer is determined by the source Transmit Path Overhead Processor (TPOP). The path overhead is inserted by the source TPOP and is passed transparently across the APS interface.

When the APS interface is carrying a receive path being protected, the pointer is determined by the receive pointer value and the frequency offset between the reference clock REFCLK and the receive serial interface. The STAL blocks perform pointer manipulation to ensure the payload and path overhead are passed transparently.

Figure 17 APS Mapping into the STS-3c/STM-1 SPE



13.1.4 Transport and Path Overhead Bytes

Under normal operating conditions, the S/UNI-1x155 processes a subset of the complete transport overhead present in an STS-3c/STM-1 stream. The byte positions processed by the S/UNI-1x155 are indicated in Figure 18.

Figure 18 STS-3c/STM-1 Overhead

STS-3c Transport Overhead
STM-1 Section Overhead

A1	A1	A1	A2	A2	A2	J0	Z0	Z0
B1			E1			F1		
D1			D2			D3		
H1	H1	H1	H2	H2	H2	H3	H3	H3
B2	B2	B2	K1			K2		
D4			D5			D6		
D7			D8			D9		
D10			D11			D12		
S1	Z1	Z1	Z2	Z2	M1	E2		

13.1.5 Transport Overhead Bytes

A1, A2: The frame alignment bytes (A1, A2) locate the SONET/SDH frame in the STS-3c/STM-1 serial stream.

J0: The J0 byte is currently defined as the STS-3c/STM-1 section trace byte for SONET/SDH. J0 byte is not scrambled by the frame synchronous scrambler.

Z0: The Z0 bytes are currently defined as the STS-3c/STM-1 section growth bytes for SONET/SDH. Z0 bytes are not scrambled by the frame synchronous scrambler.

B1: The section bit interleaved parity byte provides a section error monitoring function.

In the transmit direction, the S/UNI-1x155 calculates the B1 byte over all bits of the previous frame after scrambling. The calculated code is then placed in the current frame before scrambling.

In the receive direction, the S/UNI-1x155 calculates the B1 code over the current frame and compares this calculation with the B1 byte received in the following frame. B1 errors are accumulated in an error event counter.

D1 - D3: The section data communications channel provides a 192 kbit/s data communications channel for network element to network element communications.

In the transmit direction, the section DCC byte is inserted from a dedicated 192 kbit/s input, TDCC, when the channel is configured for section DCC.

In the receive direction, the section DCC is extracted on a dedicated 192 kbit/s output, RDCC, when the channel is configured for section DCC.

H1, H2: The pointer value bytes locate the path overhead column in the SONET/SDH frame.

In the transmit direction, the S/UNI-1x155 inserts a fixed pointer value, with a normal new data flag indication in the first H1-H2 pair. The concatenation indication is inserted in the remaining H1-H2 pairs (STS-3c/STM-1). Pointer movements can be induced using the TPOP registers.

In the receive direction, the pointer is interpreted to locate the SPE. The loss of pointer state is entered when a valid pointer cannot be found. Path AIS is detected when H1, H2 contain an all ones pattern.

H3: The pointer action bytes contain synchronous payload envelope data when a negative stuff event occurs. The all zeros pattern is inserted in the transmit direction. This byte is ignored in the receive direction unless a negative stuff event is detected.

B2: The line bit interleaved parity bytes provide a line error monitoring function.

In the transmit direction, the S/UNI-1x155 calculates the B2 values. The calculated code is then placed in the next frame.

In the receive direction, the S/UNI-1x155 calculates the B2 code over the current frame and compares this calculation with the B2 code receive in the following frame. Receive B2 errors are accumulated in an error event counter.

K1, K2: The K1 and K2 bytes provide the automatic protection switching channel. The K2 byte is also used to identify line layer maintenance signals. Line RDI is indicated when bits 6, 7, and 8 of the K2 byte are set to the pattern '110'. Line AIS is indicated when bits 6, 7, and 8 of the K2 byte are set to the pattern '111'.

In the transmit direction, the S/UNI-1x155 provides register control for the K1 and K2 bytes.

In the receive direction, the S/UNI-1x155 provides register access to the filtered APS channel. Protection switch byte failure alarm detection is provided. The K2 byte is examined to determine the presence of the line AIS, or the line RDI maintenance signals

D4 - D12: The line data communications channel provides a 576 kbit/s data communications channel for network element to network element communications.

In the transmit direction, the line DCC byte is inserted from a dedicated 576 kbit/s input, TDCC, when the channel is configured for line DCC.

In the receive direction, the line DCC is extracted on a dedicated 576 kbit/s output, RDCC, when the channel is configured for line DCC.

S1: The S1 byte provides the synchronization status byte. Bits 5 through 8 of the synchronization status byte identifies the synchronization source of the STS-3c/STM-1 signal. Bits 1 through 4 are currently undefined.

In the transmit direction, the S/UNI-1x155 provides register control for the synchronization status byte.

In the receive direction, the S/UNI-1x155 provides register access to the synchronization status byte. The SSTB block also provides circuitry to detect synchronization status mismatch and unstable alarms.

Z1: The Z1 bytes are located in the second and third STS-1's locations of an STS-3c/STM-1 and are allocated for future growth.

M1: The M1 byte is located in the third STS-1 locations of a STS-3c/STM-1 and provides a line far end block error function for remote performance monitoring.

Z2: The Z2 bytes are located in the first and second STS-1's locations of a STS-3c/STM-1 and are allocated for future growth.

In the transmit direction, Z2 byte is internally generated. The number of B2 errors detected in the previous interval is inserted.

In the receive direction, a legal Z2 byte value is added to the line FEBE event counter.

13.1.6 Path Overhead Bytes

J1: The Path Trace byte is used to repetitively transmit a 64-byte CLLI message (for SONET/SDH networks), or a 16-byte E.164 address (for SDH networks). When not used, this byte should be set to transmit continuous null characters. Null is defined as the ASCII code, 0x00.

In the transmit direction, characters can be inserted using the TPOP Path Trace register or the SPTB block. The register is the default selection and resets to 0x00 to enable the transmission of NULL characters from a reset state.

In the receive direction, the path trace message is optionally extracted into the 16 or 64 byte path trace message buffer.

B3: The path bit interleaved parity byte provides a path error monitoring function.

In the transmit direction, the S/UNI-1x155 calculates the B3 bytes. The calculated code is then placed in the next frame.

In the receive direction, the S/UNI-1x155 calculates the B3 code and compares this calculation with the B3 byte received in the next frame. B3 errors are accumulated in an error event counter.

C2: The path signal label indicator identifies the equipped payload type. For ATM payloads, the identification code is 0x13. For Packet over SONET/SDH (including $X^{43}+1$ payload scrambling), the identification code is 0x16.

In the transmit direction, the S/UNI-1x155 inserts the value 0x13 or 0x16 using the TPOP Path Signal Label register.

In the receive direction, the code is available in the RPOP Path Signal Label register. In addition, the SPTB block also provides circuitry to detect path signal label mismatch and unstable alarms.

G1: The path status byte provides a path FEBE function, and a path remote defect indication function. Three bits are allocated for remote defect indications: bit 5 (the path RDI bit), bit 6 (the auxiliary path RDI bit) and bit 7 (Enhanced RDI bit). Taken together these bits provide a eight state path RDI code that can be used to categorize path defect indications.

In the transmit direction, the S/UNI-1x155 provides register bits to control the path RDI (bit 5) and auxiliary path RDI (bit 6) states. For path FEBE, the number of B3 errors detected in the previous interval is inserted either automatically or using a register. This path FEBE code has 9 legal values, namely 0 to 8 errors.

In the receive direction, a legal path FEBE value is accumulated in the path FEBE event counter. In addition, the path RDI and auxiliary path RDI signal states are available in internal registers.

H4: The multi-frame indicator byte is a payload specific byte, and is not used for ATM payloads. This byte is forced to 0x00 in the transmit direction, and is ignored in the receive direction.

Z3 - Z5: The path growth bytes provide three unused bytes for future use.

In the transmit direction, the growth bytes may be inserted from the three TPOP Path Growth byte registers.

13.2 UTOPIA Level 2 ATM Cell Data Structure

ATM cells may be passed to/ from the S/UNI-155 using a 27 word, 16-bit/8bit UTOPIA level 2 compliant data structure. The 16-bit data structure is shown in Figure 19and described below.

Figure 19 16-bit Wide, 27 Word ATM Cell Structure

	Bit 15 Bit 8	Bit 7 Bit 0
Word 1	H1	H2
Word 2	H3	H4
Word 3	H5	HCS Status/Control
Word 4	Payload 1	Payload 2
Word 5	Payload 3	Payload 4
Word 6	Payload 5	Payload 6
Word 7	Payload 7	Payload 8
Word 8	Payload 9	Payload 10
	⋮	⋮
Word 27	Payload 47	Payload 48

Bit 15 of each word is the most significant bit (which corresponds to the first bit transmitted or received). The header check sequence octet (HCS) is passed through this structure. The start of cell indication input and output (TSOC and RSOC) are coincident with Word 1 (containing the first two header octets). Word 3 of this structure contains the HCS octet in bits 15 to 8.

In the receive direction, the lower 8 bits of Word 3 contain the HCS status octet. An all-zeros pattern in these 8 bits indicates that the associated header is error free. An all-ones pattern indicates that the header contains an uncorrectable error (if the HCSPASS bit in the RXCP Control Register is set to logic zero, the all-ones pattern will never be passed in this structure). An alternating ones and zeros pattern (0xAA) indicates that the header contained a correctable error. In this case the header passed through the structure is the "corrected" header.

In the transmit direction, the HCS bit in the TXCP Control register determines whether the HCS is calculated internally or is inserted directly from the upper 8 bits of Word 3. The lower 8 bits of Word 3 contain the HCS control octet. The HCS control octet is an error mask that allows the insertion of one or more errors in the HCS octet. A logic one in a given bit position causes the inversion of the corresponding HCS bit position (for example a logic one in bit 7 causes the most significant bit of the HCS to be inverted). The HDCL control octet may be disabled by setting the HCSCTLEB register in the TXCP.

13.3 POS-PHY Level 2 Data Structures

Packets may be written into the TXFP FIFO and read from the RXFP FIFO using a 16-bit POS-PHY Level 2 defined data structure.

The 16-bit POS-PHY Level 2 data structure is shown in Figure 20. The packet length of 63 bytes is chosen arbitrarily for illustrative purposes only. Other lengths are acceptable. Octets are written in the same order they are to be transmitted or they were received on the SONET/SDH line. Within an octet, the MSB (bit 7) is the first bit to be transmitted. All words are composed of two octets, except the last word of a packet which can have one or two bytes. If the TXFP is configured to not insert the FCS field, then these bytes should be included at the end of the packet. Similarly, if the RXFP is configured to not strip the FCS field, then these bytes will be included at the end of the packet.

Figure 20 A 63 Byte Packet Data Structure

	Bit 15 — Bit 8	Bit 7 — Bit 0
Word 1	Byte 1	Byte 2
Word 2	Byte 3	Byte 4
Word 3	Byte 5	Byte 6
Word 4	Byte 7	Byte 8
Word 5	Byte 9	Byte 10
Word 6	Byte 11	Byte 12
Word 7	Byte 13	Byte 14
	⋮	⋮
Word 32	Byte 63	XX

A 63 Byte Frame

13.4 Setting ATM Mode of Operation

Use the following sequence to prepare the device for the ATM operation.

1. Input pin POS_ATMB should be tied low to enable ATM operation.

2. Reset the device. This can be done by asserting the RSTB pin or setting the RESET bit in the Master Reset and ID Register (Register 0x000).

3. Reset and configure the CSU (Register 0x102).

4. If the TFCLK and RFCLK clock inputs are not stable clocks, wait until these clock inputs stabilize. Reset the DLL units associated with each clock input (write 0x00 to registers 0x10A and 0x10E respectively).

5. Reset the receive and transmit FIFOs by setting the FIFORST register bits in the TXCP (0x080) and RXCP (0x062) blocks. Keep these bits set for at least 1 µs, then set the bit back to its inactive logic zero value.

6. Set the path signal label C2 byte (0x048) to 0x13 to identify ATM payload data. The expected path signal label in 0x054 should also be set to 0x13.

7. Set the HCSCTLEB bit in register 0x081 to logic one to prevent corruption of the HCS byte.

8. Reset the performance monitoring counters in the TXCP and RXCP block by writing a logic zero to the Master Reset and Identity register (Register 0x000). TIP remains high as the performance monitoring registers are loaded and is set to a logic zero when the transfer is complete.

13.5 Setting Packet-Over-SONET/SDH Mode of Operation

Use the following sequence to prepare the device for the Packet over SONET/SDH (POS) operation.

1. Input pin POS_ATMB should be tied high to enable POS operation.

2. Reset the device. This can be done by asserting the RSTB pin or setting the RESET bit in the Master Reset and ID Register (Register 0x000).

3. Reset and configure the CSU (Register 0x102).

4. If the TFCLK and RFCLK clock inputs are not stable clocks, wait until these clock inputs stabilize. Reset the DLL units associated with each clock input (write 0x00 to registers 0x10A and 0x10E respectively).

5. Reset the receive and transmit FIFOs by setting the FIFORST register bits in the TXCP (0x080) and RXCP (0x062) blocks. Keep these bits set for at least 1 µs, then set the bit back to its inactive logic zero value.

6. Set the path signal label C2 byte (0x048) to 0x16 to identify POS payload data.

7. Reset the performance monitoring counters by writing a logic zero to the Master Reset and Identity register (Register 0x000). TIP remains high as the performance monitoring registers are loaded, and is set to a logic zero when the transfer is complete.

13.6 Setting SONET or SDH Mode of Operation

The SONET and SDH standard for optical networking are very similar with only minor difference in overhead processing. The main difference between the SONET (Bellcore GR-253-CORE) and SDH (ITU.707) standards lies in the handling of some of the overhead bytes. Other details, like framing and data payload mappings are equivalent in SONET and SDH.

The bit error rate (BER) monitoring requirements are also slightly different between SONET and SDH. An application note, PMC-950820, explains the different parameters in detail for the RASE block.

The list below shows the various register settings to configure the S/UNI-1x155 for either SONET or SDH operation.

Table 16 Settings for SONET or SDH Operation

Configuration Registers	SONET	SDH
SDH_J0/Z0 (register 0x004)	0	X
ENSS (register 0x03D)	0	1
Path LEN16 (register 0x028)	0	1
Section LEN16 (register 0x050)	0	1
S[1:0] (register 0x046)	00	10

Notes:

1. SONET requires Z0 bytes to be set to the number corresponding to the STS-1 column number. SDH considers those bytes reserved.
2. When forcing a constant Z0 pattern (SDH_J0/ZO is high), the Z0 bytes must be DC balanced (approximately the same number of ones and zeros) as the bytes are not scrambled. Failure to do so may cause downstream clock recovery to lose lock.
3. SONET uses 64 byte trace messages while SDH uses 16 byte trace messages.
4. SDH specification requires the detector of SS bits to be “10”.
5. The SS bits are undefined for SONET, but must be set to “10” for SDH.

13.7 Bit Error Rate Monitor

The S/UN-1x155 provides two BERM blocks. One can be dedicated to monitor at the Signal Degrade (SD) error rate and the other dedicated to monitor at the Signal Fail (SF) error rate.

The Bit Error Rate Monitor (BERM) block counts and monitors line BIP errors over programmable periods of time (window size). It can monitor to declare an alarm or to clear it if the alarm is already set. A different threshold and accumulation period must be used to declare or clear the alarm, whether or not those two operations are not performed at the same BER. The following table lists the recommended content of the BERM registers for different error rates (BER). Both BERMs in the TSB are equivalent and are programmed similarly. In a normal application they will be set to monitor different BER.

When the SF/SD CMODE bit is set to one, the clearing monitoring is recommended to be performed using a window size that is 8 times longer than the declaration window size. When the SF/SD CMODE bit is set to zero, the clearing monitoring is recommended to be performed using a window size equal to the declaration window size. In all cases, the clearing threshold is calculated for a BER that is 10 times lower than the declaration BER, as required in the references. The table indicates the declare BER and evaluation period only.

The saturation threshold is not listed in the table, and should be programmed with the value 0xFFF by default, deactivating saturation. Saturation capabilities are provided to allow the user to address issues associated with error bursts.

For additional information, please refer to the BERM application note (PMC-1950820) for more detailed information.

Table 17 Recommended BERM settings

STS	Declare BER	Evals / Second	SF/SD SMODE	SF/SD CMODE	SF/SD SAP	SF/SD DTH	SF/SD CTH
STS-3c	10^{-3}	0.008	0	0	0x000008	0x245	0x083
STS-3c	10^{-4}	0.013	0	1	0x00000D	0x0A3	0x0B4
STS-3c	10^{-5}	0.100	0	1	0x000064	0x084	0x08E
STS-3c	10^{-6}	1.000	0	1	0x0003E8	0x085	0x08E
STS-3c	10^{-7}	10.000	0	1	0x002710	0x085	0x08E
STS-3c	10^{-8}	83.000	0	1	0x014438	0x06D	0x077
STS-3c	10^{-9}	667.000	0	1	0x0A2D78	0x055	0x061

13.8 Auto Alarm Control Configuration

The S/UNI-1x155 supports the automatic generation of transmit alarm information based on the detected receive alarms. This functionality is controlled by the master AUTOxx register bits in channel register 0x005 and the Auto Path and Line Configuration channel registers 0x008 to 0x00F.

When consequential action is enabled for a given alarm condition, other S/UNI-1x155 configuration registers become important. For instance, if consequential action for signal degrade is enabled, the RASE must be configured for the desired alarm thresholds. The following table lists register settings for path RDI and extended path RDI interfaces.

Table 18 Path RDI and Extended RDI Register Settings

Offset	RDI	EPRDI
0x009	11111111	01101111
0x00A	xxxxxxxx	11111111
0x00B	10xxx010	11xxx111
0x040	x00x00xx	x11x00xx

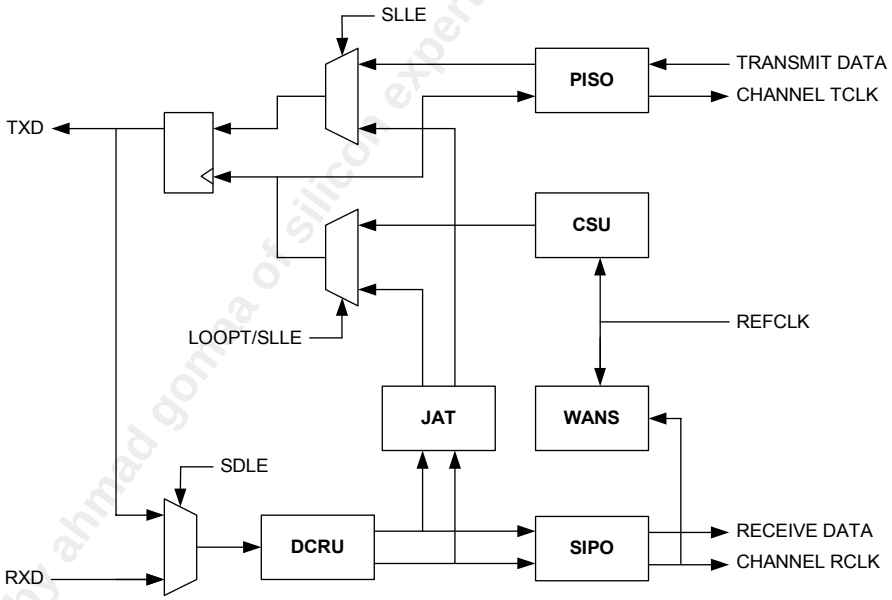
Since the same receive path processor (RPOP) is used no matter the setting of the receive APS enable RXEN (selecting working or protection channel), path alarm and FEBE information is passed from the RPOP to the TPOP in the device.

13.9 Clocking Options

The S/UNI-1x155 supports several clocking modes. Figure 21 is an abstraction of the clocking topology. The S/UNI-1x155 can operate in source time, internally loop timed and externally loop timed.

Source timed operation is used for all public user network interfaces (UNIs) and for private UNIs and private network node interfaces (NNIs) that are not synchronized to the recovered clock.

Figure 21 Clocking Structure



The transmit clock in a public UNI must conform to SONET/SDH Network Element (NE) requirements specified in Bellcore GR-253-CORE. These requirements include jitter generation, short term clock stability, phase transients during synchronization failure, and holdover. The 19.44 MHz clock source is typically a VCO (or temperature compensated VCXO) locked to a primary reference source for public UNI applications. The accuracy of this clock source should be within ±20 ppm of 19.44 MHz to comply with the SONET/SDH network element free-run accuracy requirements. The S/UNI-1x155 WANS block can be used to implement the system timing reference.

The transmit clock in a private UNI or a private NNI may be locked to an external reference or may free-run. The simplest implementation requires an oscillator free-running at 19.44 MHz.

Source timed operation is selected by clearing the LOOPT bit of the channel's Master Configuration register. REFCLK is multiplied by 8 to become the 155.52 MHz transmit clock. REFCLK must be jitter free. The source REFCLK is also internally used as the clock recovery reference during receive loss of transition conditions.

Internally loop timed operation is used for private UNIs and private NNIs that require synchronization to the recovered clock. This mode is selected by setting the LOOPT bit of the channel's Master Configuration register to logic one. Normally, the transmit clock is locked to the receive data. In the event of a loss of signal/transition condition, the transmit clock is synthesized from REFCLK.

Externally loop timed operation makes use of the WAN Synchronization block capabilities. This mode can be achieved when LOOPT is set to logic zero. The timing loop is achieved at the system level, through a microprocessor, an external VCXO and back through the REFCLK input. This mode allows an S/UNI-1x155 to meet Bellcore wander transfer and holdover stability requirements.

13.10 WAN Synchronization (WANS Block)

The WANS provides a means to implement a Stratum 3 or lower system timing reference with a minimum amount of external circuitry. The WANS implements a phase detector necessary to create a digital control PLL.

A description of how to program and use the WANS feature can be found in the TETRA reference design (PMC-1980322).

13.11 Loopback Operation

The S/UNI-1x155 supports five loopback functions: path loopback, line loopback, data diagnostic loopback, parallel diagnostic loopback and serial diagnostic loopback. Each channel's loopback modes operate independently. The loopback modes are activated by the PDLE, SLLE, DLE, DPLE and SDLE bits contained in the channel's Master Configuration registers.

The line loopback, see Figure 22, connects the high speed receive data and clock to the high speed transmit data and clock, and can be used for line side investigations (including clock recovery and clock synthesis). While in this mode, the entire receive path is operating normally and cells can be received through the FIFO interface.

The serial diagnostic loopback, see Figure 23, connects the high speed transmit data and clock to the high speed receive data and clock. While in this mode, the entire transmit path is operating normally and data is transmitted on the TXD+/- outputs.

The parallel diagnostic loopback, see Figure 24, connects the byte wide transmit data and clock to the byte wide receive data and clock. While in this mode, the entire transmit path is operating normally and data is transmitted on the TXD+/- outputs.

The path diagnostic loopback, see Figure 25, connects the transmit path processor TPOP output to the receive path processor RPOP. While in this mode, the entire transmit path is operating normally and data is transmitted on the TXD+/- outputs.

The data diagnostic loopback, see Figure 26, connects the transmit POS/ATM processor TXFP/TXCP) to the corresponding receive POS/ATM processor (RXFP/RXCP). While in this mode, the transmit path does not operate normally and the data transmitted on the TXD+/- outputs is invalid.

Figure 22 Line Loopback Mode

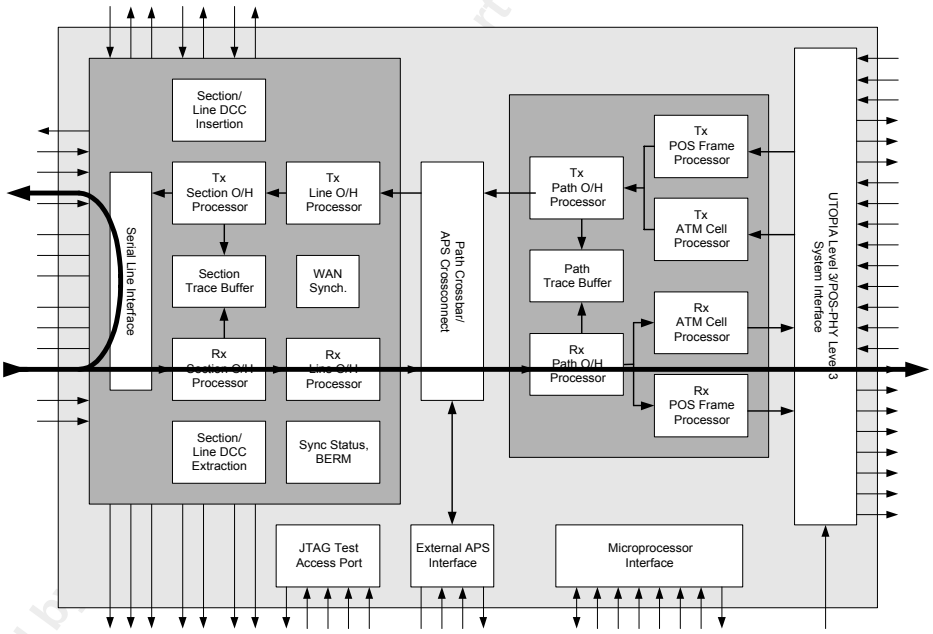


Figure 23 Serial Diagnostic Loopback Mode

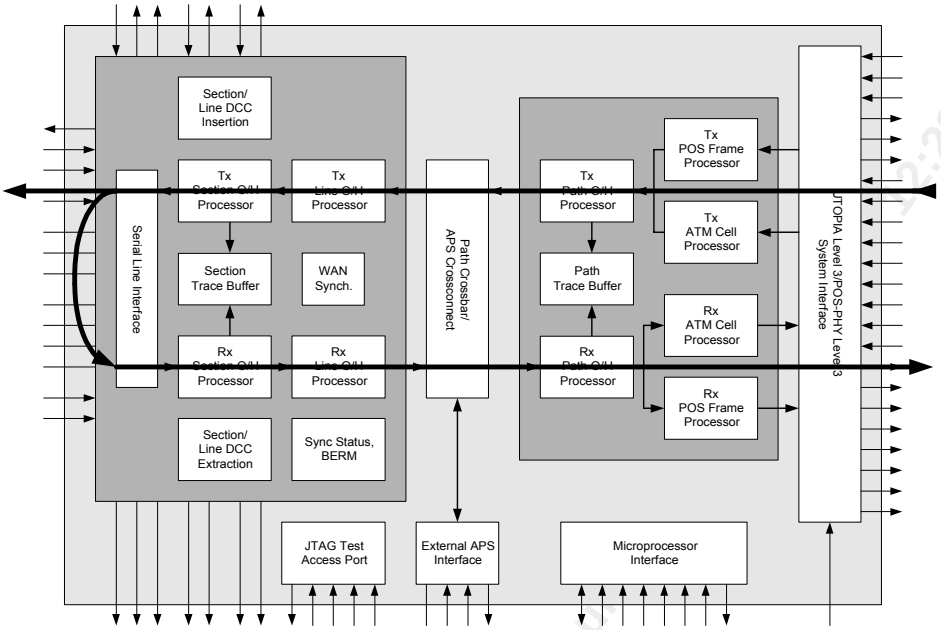


Figure 24 Parallel Diagnostic Loopback Mode

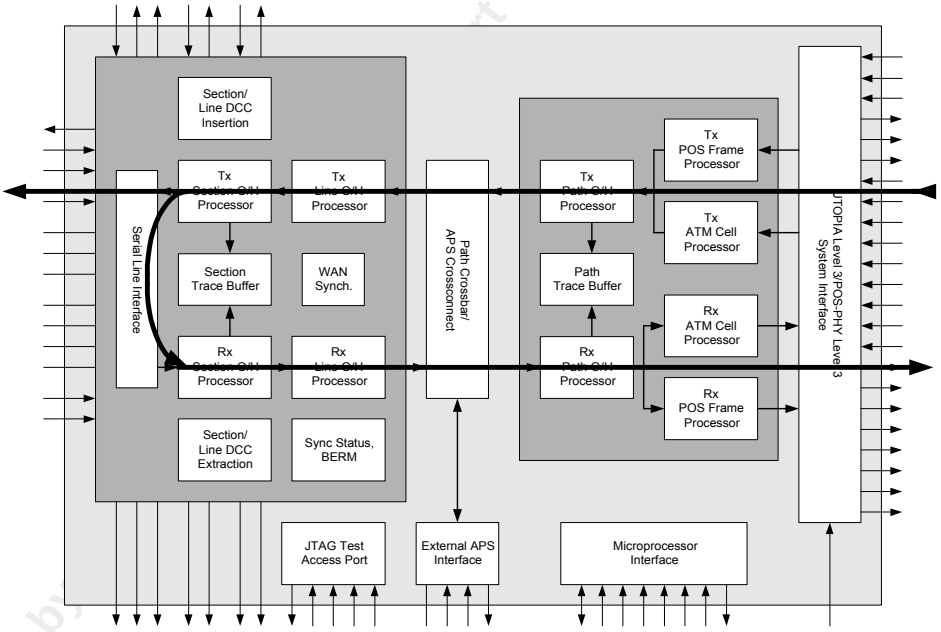


Figure 25 Path Diagnostic Loopback Mode

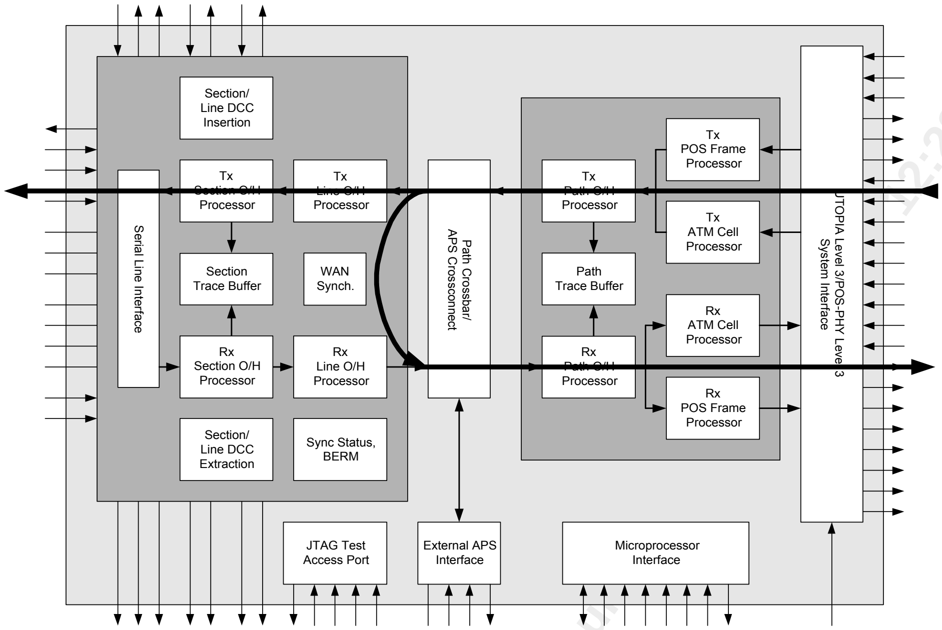
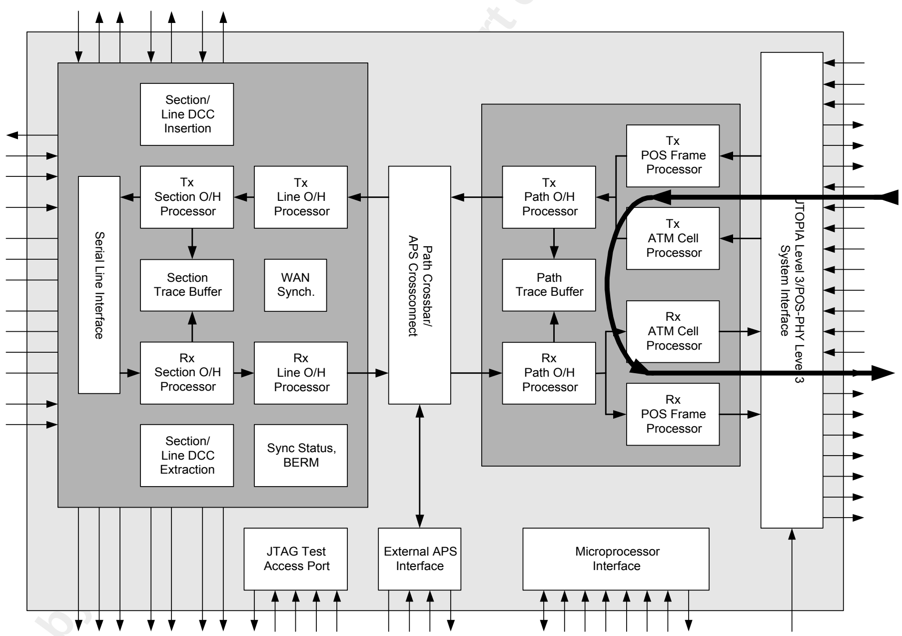


Figure 26 Data Diagnostic Loopback Mode

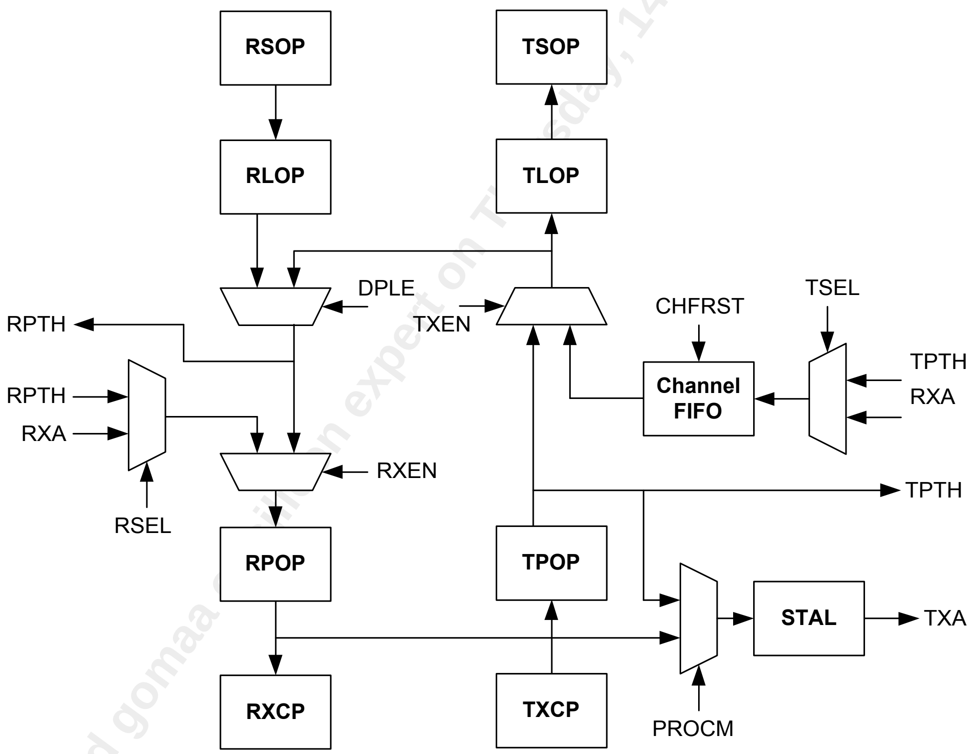


13.12 APS Support

The S/UNI-1x155 has the ability to exchange transmit path data with another S/UNI-1x155 in order to implement APS interface. The APS support logic may also be used to reassign at the path level the channel number in a single S/UNI-1x155. The diagram in Figure 27 shows the APS support logic. The diagnostic path loop back DPLE is shown to illustrate that path loop back includes all path functions including the APS stream if used.

In the transmit direction, the transmit path may be configured using the TXEN register to use the normal transmit path from TPOP or the APS path stream. The channel adds section and line overhead to the transmit path data stream using its TSOP and TLOP units. Thus, each channel has unique K1/K2 byte control.

Figure 27 Channel APS Structure

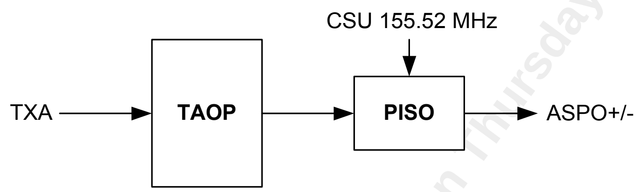


In the receive direction, channel processes section and line overhead in the receive path stream using its RSOP and RLOP units. Thus, each channel has unique K1/K2 byte monitoring. The receive path may be configured using the RXEN register to use the normal receive path from RLOP or the APS path stream. The channel path processors, RPOP and TPOP, are connected for AUTOPRDI and FEBE functionality.

The 8-byte channel FIFO is used to handle fixed phase variations between channels caused by the serial line interface PISO blocks. Each PISO generates an upstream TCLK from the serial transmit clock using a free running divide-by-8 counter. Since each PISO can generate a TCLK which is exactly the same frequency, but with a different phase offset, the channel FIFO is used to cross clock domains between channels. The channel FIFO should reset using CHFRST to center the read and write pointers when the APS link is configured.

The diagram in Figure 28 shows the structure of a transmit APS link. The channel may be configured using the PROCM register (in Figure 27) to send receive path information or transmit path information over the APS link. The transmit APS link has a one-to-one correlation between channel and APS link. That is, the channel's APS information is passed to the other S/UNI-1x155 device on a fixed APS link. The TAOP block performs BIP calculation and SONET scrambling functions for the transmit APS stream. The PISO block generates the 155.52 Mbit/s serial stream for the interface.

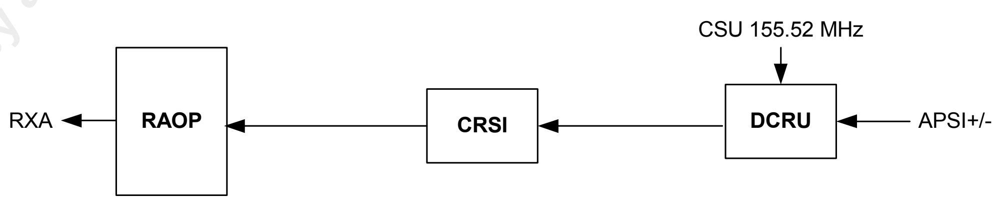
Figure 28 Transmit APS Link



When passing receive path over the transmit APS link, the STAL block performs pointer processing to handle frequency offsets and jitter variations between the recovered clock and the synthesized 155.52 MHz clock from the CSU. In order to process the pointer, the RPOP block must interpret the STS-3c/STM-1 pointer for the STAL block. When the receive path stream becomes invalid (due to various SONET alarms including LOP, LOS, PAIS, LOPC, AISC), path AIS is forced over the transmit APS link.

The diagram in Figure 29 shows the structure of a receive APS link. The receive APS link uses a DCRU to recover the data from the incoming 155Mbit/s stream. The DCRU will track high frequency jitter and low frequency wander of the incoming serial stream. The APS FIFO is used to handle the phase variation between the APS serial stream and the synthesized 155.52 MHz clock from the CSU which is used to generate the transmit serial data stream. The APS DCRU interrupt DCRUI will indicate when the DCRU tries to move beyond either end of the delay line.

Figure 29 Receive APS Link



Because of the architecture of the receive APS interface, the reference clocks REFCLK for both S/UNI-1x155 must be frequency locked. While the DCRU can track jitter on the serial interface, the DCRU cannot process serial interfaces with a frequency offset from the 155.52 MHz clock synthesized by the CSU block.

The RAOP and SIPO blocks perform SONET framing, BIP calculation and performance monitoring. The DCC channel is used to carry transport alarm status (LOS, LOF, and LAIS) of the path streams in order for the AUTOPRDI logic to quickly respond to these alarms. While the transport alarm status is not necessary to generate correct PRDI in the transmit direction, the transport alarm status allows the AUTOPRDI to quickly report PRDI without waiting numerous SONET frames for the receive RPOP to declare path failure.

Table 19 describes basic programming requirements for 1+1 APS configuration. See also Figure 29 for more information about the Channel APS Structure and the Configuration Register Bits.

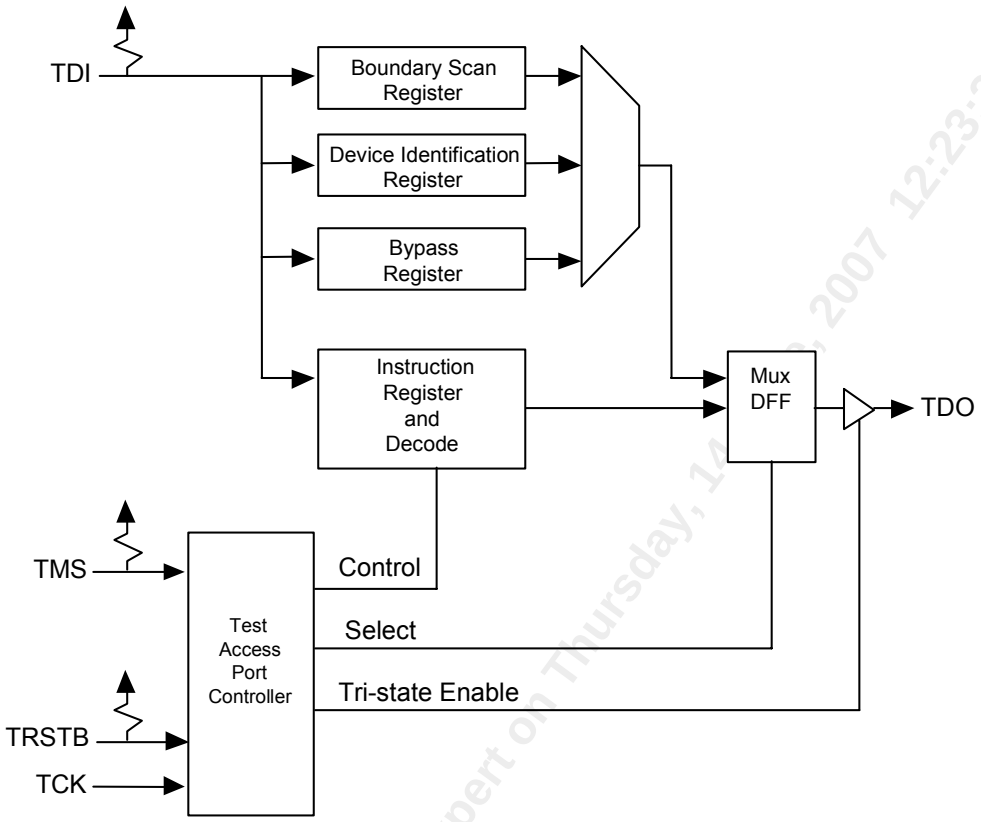
Table 19 1+1 APS Configuration

Configuration Register Bits	Protection Device APS Configuration	Working Device APS Configuration
RXEN	1	0
RSEL	1	don't care
TXEN	1	0
TSEL	1	don't care
PROCM	0	1

13.13 JTAG Support

The S/UNI-1x155 supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins, TRSTB, TCK, TMS, TDI and TDO used to control the TAP controller and the boundary scan registers. The TRSTB input is the active-low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown below.

Figure 30 Boundary Scan Architecture



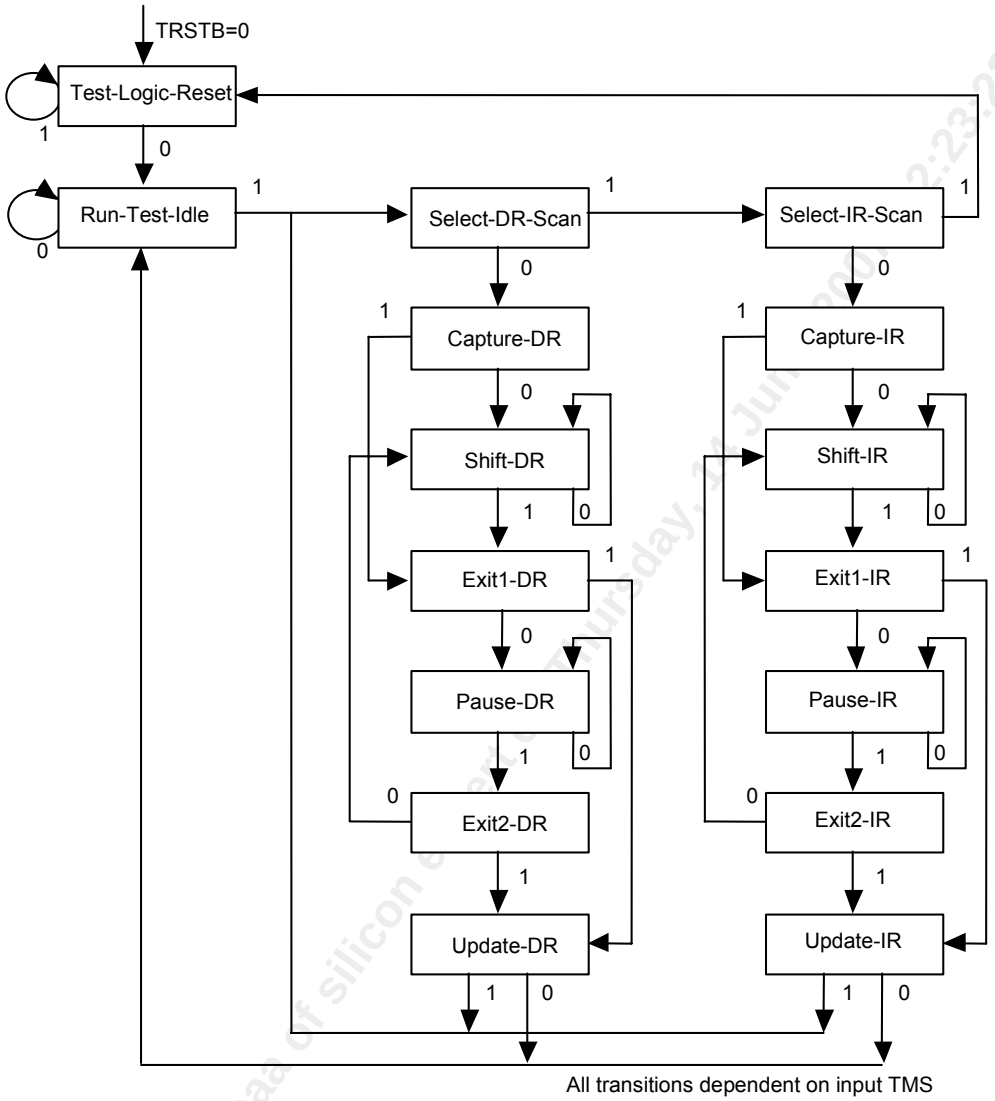
The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single-bit delay from primary input, TDI to primary output, TDO. The device identification register contains the device identification code.

The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register place in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be sampled and shifted out on primary output, TDO. In addition, patterns can be shifted in on primary input, TDI and forced onto all digital outputs.

13.13.1 TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is shown in Figure 31.

Figure 31 TAP Controller Finite State Machine



13.13.2 States

Test-Logic-Reset

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

Run-Test-Idle

The run test/idle state is used to execute tests.

Capture-DR

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-IR

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

13.13.3 Boundary Scan Instructions

The following is a description of the standard instructions. Each instruction selects a serial test data register path between input, TDI and output, TDO.

BYPASS

The bypass instruction shifts data from input, TDI to output, TDO with one TCK clock period delay. The instruction is used to bypass the device.

EXTEST

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is placed between input, TDI and output, TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCODE

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

STCTEST

The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out output, TDO using the Shift-DR state.

13.14 Board Design Recommendations

The noise environment and signal integrity are often the limiting factors in system performance. Therefore, the following board design guidelines must be followed in order to ensure proper operation:

- Use a single plane for both digital and analog grounds.
- Provide separate +3.3 volt analog and +3.3 volt digital supplies, but otherwise connect the supply voltages together at one point close to the connector where +3.3 volts is brought to the card.
- Ferrite beads are not advisable in digital switching circuits because inductive spiking (di/dt noise) is introduced into the power rail. Simple RC filtering is the best approach provided care is taken to ensure the IR drop in the resistance does not lower the supply voltage below the recommended operating voltage.
- High-frequency decoupling capacitors are recommended for each power pin as close to the package pin as possible. Separate decoupling is required to prevent the transmitter from coupling noise into the receiver and to prevent power supply transients from coupling into some internal reference circuitry. See the section on Power Supplies for more details.

- Low-pass filtering networks are recommended for analog power supplies as close to the package pin as possible. Separate decoupling is required to prevent the transmitter from coupling noise into the receiver and to prevent power supply transients from coupling into some internal reference circuitry. See the section on Power Supplies for more details.
- The high speed serial streams (TXD+/- and RXD+/-) must be routed with 50 ohm controlled impedance circuit board traces and must be terminated with a matched load. Normal TTL-type design rules are not recommended and will reduce the performance of the device. See the section on interfacing to ECL and PECL devices for more details.

13.15 Power Supplies

Due to ESD protection structures in the pads it is necessary to exercise caution when powering a device up or down. ESD protection devices behave as diodes between power supply pins and from I/O pins to power supply pins. Under extreme conditions it is possible to blow these ESD protection devices or trigger latch up. The recommended power supply sequencing follows:

1. For proper digital I/O performance, the VDDO and VDDQ supplies should be the same source.

2. The VDDO/VDDQ supplies must be applied before or at the same time as QAVD and AVD supplies (the voltage difference between any two pins must be less than 0.5 volts) or the QAVD and AVD supplies must be current limited to the maximum latch-up current specification.

3. VDDI supplies must be applied after VDDO/VDDQ has been applied or must be current limited to the maximum latch-up current specification.

4. VDDO/VDDQ/VDDI supplies must be applied before digital input pins are driven or the current per pin limited to less than the maximum DC input current specification.

5. AVD supplies must be applied before analog input pins are driven or the current per pin limited to less than the maximum DC input current specification.

6. The differential voltage between VDDO/VDDQ and AVD must be less than 1.0 volts including peak to peak noise. The differential voltage between VDDO and QAVD must be less than 0.5 volts including peak to peak noise. Otherwise, digital noise on VDD will be coupled into the sensitive analog circuitry.

7. Power down the device in the reverse sequence. Use the above current limiting technique for the analog power supplies. Small offsets in VDDO / VDDQ / AVD / VDDI discharge times will not damage the device.

In order to optimize jitter generated by the CSU and the jitter tolerance of the CRU, we recommend the following power filter scheme shown in Figure 32. Sensitive analog power pins require RC filter networks in order to meet SONET/SDH jitter specifications. Some recommended notes follows:

1. Place each 0.1 µF capacitor as close to its associated power pin as possible.

2. The 0.1 µF capacitors are ceramic X7R or X5R.

3. The 10 µF capacitors are 10V X5R ceramic, 1210 size, from Tayio-Yuden, LMK325BJ106MN (visit their web site at www.t-yuden.com).

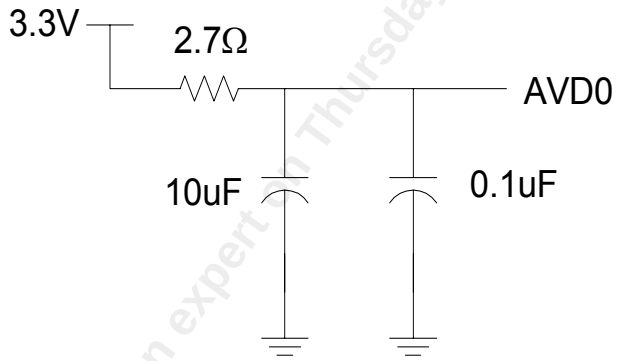
4. The 10 µF capacitors and resistors do not have to be very close to power pins as they are filtering the power supply and not decoupling it.

5. The two 10 µF X5R capacitors can be replaced by one 22uF, 10V, X5R LMK432BJ226MM from Tayio Yuden.

6. All resistors shown are 1/10 watt.

7. All other power pins not mentioned do not need any extra filtering or decoupling.

Figure 32 Power Supply Filtering and Decoupling



In addition to the circuit shown in Figure 32:

1. Place one 0.1 uF capacitor for each of the following pins (18 capacitors): QAVD (J4), AVD1 (H5), VDDO1 (C4), VDDO2 (C6), VDDO3 (C10), VDDO4 (D12), VDDO8 (F12), VDDO11 (H12), VDDO12 (K3), VDDO13 (K12), VDDO14 (M4), VDDO15 (M6), VDDO17 (M10), VDDO18 (M12), VDDI0 (C8), VDDI1 (G12), VDDI2 (F5) and VDDI3 (M7).

2. Place one 10 uF bulk decoupling capacitor near VDDI2 (F5).

3. Place one 0.1 uF decoupling capacitor for the following group of VDDO pins: G1, G3, F3, E3, E1.

4. If APS is used, add one 0.1uF capacitor for each of the following pins (2 capacitors): VDDO0 (C1) and VDDO5 (E1).

13.15.1 Increased Power Supply Noise Tolerance

To obtain a greater power supply noise immunity of up to 200 mVolts of peak to peak noise it is recommended that an AVD filter compromised of a 5R1 resistor along with a 47uF capacitor be implemented instead of filter in Figure 32.

Table 20 Power Supply Noise Tolerance

Configuration	Unit	Minimum Amplitude (mVolts)
Power Supply Noise Tolerance With the Filter in Figure 32	Vpp	150
Power Supply Noise Tolerance With The Recommended Filter (5R1 + 47uF)	Vpp	200

13.16 High Speed PECL Interfaces

In normal operation, the S/UNI-1x155 performs clock and data recovery on the incoming serial stream. The device is designed for optical modules without clock and data recovery such as HFCT/HFBR-5208 transceivers.

Only a few passive components are required to convert the optical transceivers signals to ECL (or PECL) logic levels. Figure 33 and Figure 34 illustrate the recommended configurations for both types of ECL voltage levels when connecting to optical modules. Note that the RXD+/- inputs are internally terminated with a 100 ohm resistor between the differential inputs. The SPECLV must be set appropriately to configure the RXD+/- and SD for the optical module being used. The SD also supports TTL input which may be enabled using the SDTTL input.

The TXD+/- outputs are AC coupled so that the ECL inputs of the optical module are free to swing around the ECL bias voltage (V_{BB}). In general, the ECL bias voltage is referenced 1.3volts lower than the supply. The bias voltage may be generated using a resistor divided as shown in Figure 34. The bias voltage may be shared between optical modules if the resistor divider is well decoupled and star connected to the termination networks. Otherwise, data dependent jitter may be coupled between optic modules.

The TXD+/- outputs on the S/UNI-1x155 swing approximately 3.3V and requires the combination of the series source resistor and the termination resistors to divide the output voltage down to a nominally 800mV swing. The series resistor attenuates the signal as well as damping any signal reflections from the optics module. Calculations involving the series resistor must include the 15 to 20 ohm source resistance of the TXD+/- output drivers.

The 50 ohm control impedance traces reduce the effect of signal reflections between the optical module and the S/UNI-1x155. Vias should be avoided on the signal path between the optical module and the S/UNI-1x155 as they can affect the jitter performance of the interface. Vias may be used for the termination networks as the inductive effective of a via will not significantly affect the termination performance.

Figure 33 Interfacing S/UNI-1x155 Line PECL Pins to 3.3V Devices

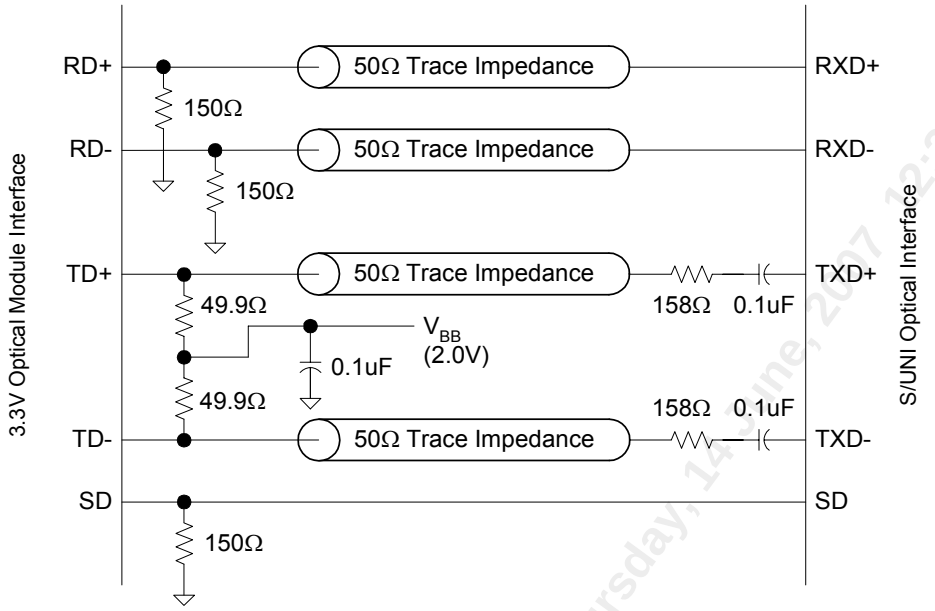


Figure 34 Interfacing S/UNI-1x155 Line PECL Pins to 5.0V Devices

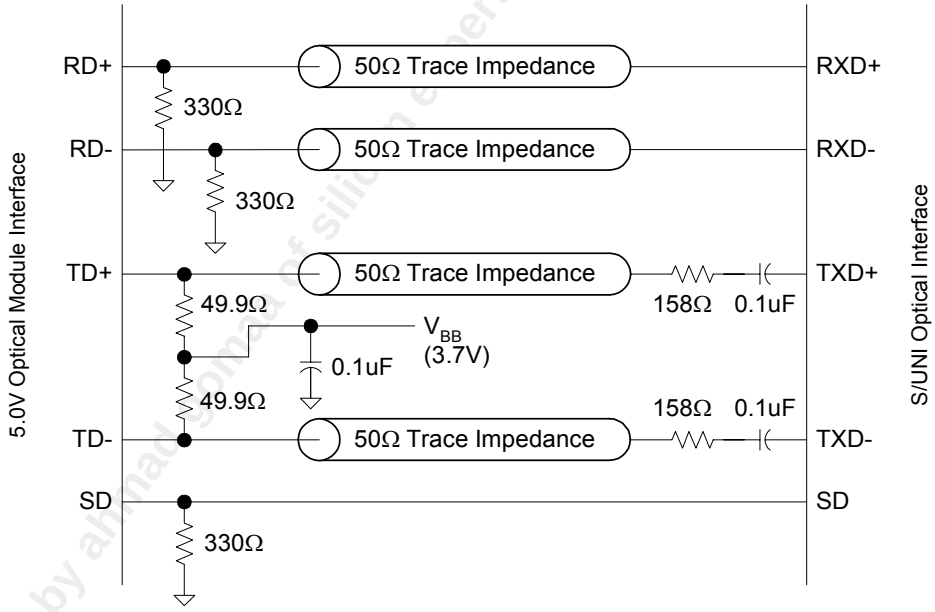
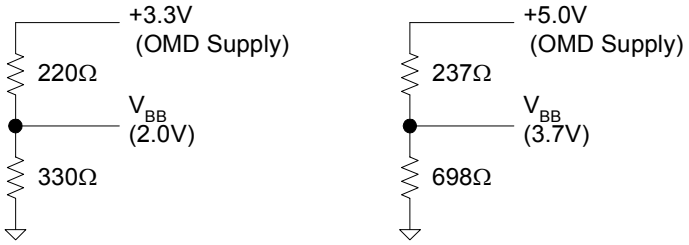


Figure 35 ECL Bias Voltage Generator Networks



The APS serial interface is designed for 155.52 MHz operation. The APECLV input controls the ECL levels for the APSI+/- inputs and APSO+/- outputs. Note that the APSI+/- inputs are internally terminated with a 100 ohm resistor between the differential inputs.

The 50 ohm control impedance traces must be less than 12 cm in length to reduce the effect of signal reflections between the two S/UNI-1x155. If the APS traces are longer than 12cm (for instance, the APS traces travel over a backplane), the APSO+/- outputs should be buffered using standard ECL buffers. The ECL buffers will ensure proper signal levels at the APSI+/- with little waveform overshoot or undershoot. Figure 36 and Figure 37 illustrate the recommended configurations for both types of ECL voltage levels when connecting to ECL buffers. Figure 38 illustrates the recommended configuration for connecting two S/UNI-1x155.

When a APSI+/- PECL input is not being used, the positive differential input must be tied to digital power (VDDO) and the negative differential input must be tied to digital ground (VSSO). In all cases, the PECL inputs must be driven with a differential voltage (do not connect both pins to VDDO or VSSO). When a APSO+/- PECL output is not being used, both the positive and negative differential outputs of the PECL output may be tied both to digital ground (VSSO).

Figure 36 APS Output Interface to PECL buffer

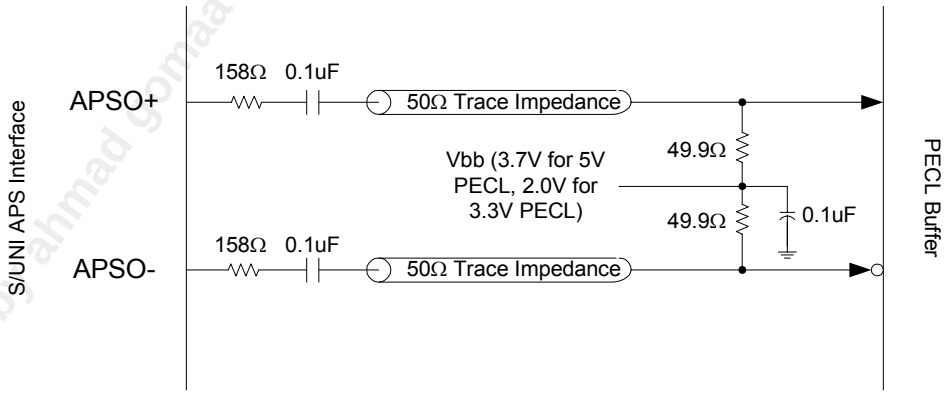


Figure 37 APS Input Interface from PECL buffer

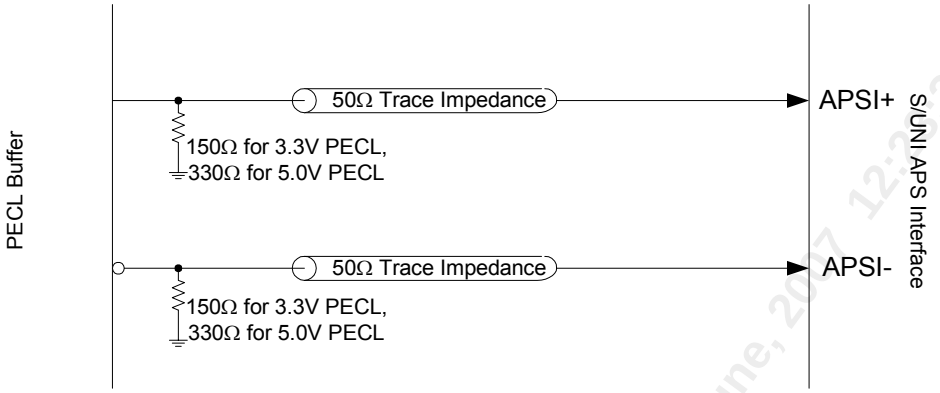
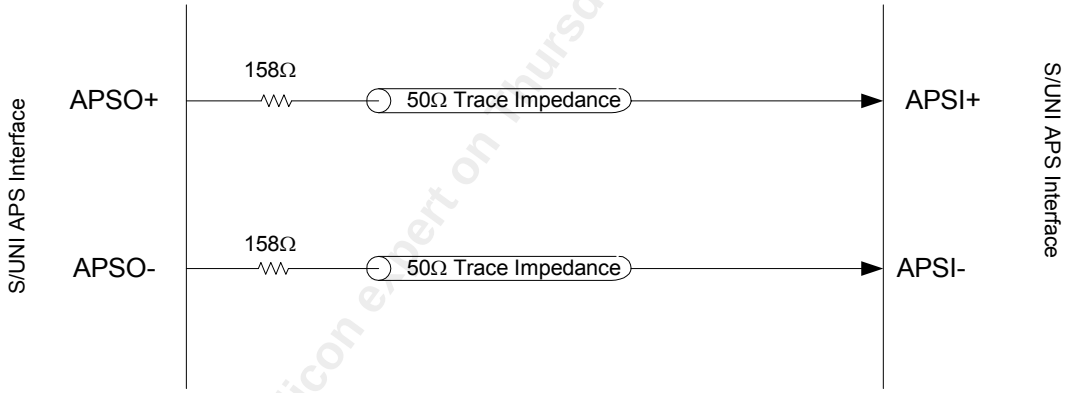


Figure 38 APS Interface between two PM5384 devices



13.17 Clock Synthesis and Recovery

The Clock Synthesizer unit (CSU) in the S/UNI-1x155 requires an external reference clock REFCLK to generate the 155.52 MHz transmit clock. In general, the reference clock REFCLK is supplied by a crystal oscillator. For more details see Table 27.

Each Clock Recovery Unit (CRU) in the S/UNI-1x155 is implemented using two digital PLL structures. The first digital PLL (DCRU) recovers the clock from the receive data RXD+/- and controls the jitter tolerance characteristics of the device. The second digital PLL (JAT) attenuates the jitter on the recovered clock and controls the jitter transfer characteristics of the device. Both PLL structures are powered from the VDDI power supply. While the digital PLLs are robust to voltage variations, the S/UNI-1x155 must be well decoupled to prevent local system voltage variations from affecting the jitter performance.

13.18 System Interface DLL Operation

The S/UNI-1x155 use digital delay lock loop (DLL) units to improve the output propagation timing on certain digital output pins. The TFCLK and RFCLK clock inputs each have a DLL to improve the timing on their associated interfaces.

The DLL compensate for internal timing and output pad delays by adaptively delaying the input clock signal by approximately one clock period (1 UI) to create a new clock which controls the internal device logic. A side effect is that the DLL units impose a minimum clock rate on each of the clock signals.

After the S/UNI-1x155 is reset, the DLL units find the initial delay lock. This process may take up to 3400 clock cycles to identify the lock position. During this initial lock period, device interface timing will not meet the timing specifications listed in A.C. Timing section. The TCA/TPA and STPA pins are held low when the TFCLK DLL is finding lock. If the clock inputs are not stable during this period (for instance, a clock is generated using an external PLL), the S/UNI-1x155 should be held in reset until the clocks are stable or the DLL should be reset using software control.

The RFCLK and TFCLK DLL software resets are performed by writing 0x00 to registers 0x10E and 0x10A respectively. When resetting the RFCLK or TFCLK DLL units, the associated FIFOs in the RXCP, RXFP, TXCP, TXCP, TFCLK DLL and RFCLK DLL blocks must also be reset using the their FIFORST register bits. The RUN register bit is set high when the DLL finds lock after a system or software reset.

The DLL units are sensitive to jitter on the clock inputs. The reason is that the DLL must track the changes in clock edges cause by changes in clock frequency, temperature, voltage and jitter. While the DLL may tolerate up to 0.4UIpp of clock jitter without losing phase lock, the output timing may degrade with excessive input jitter. Therefore, the high frequency clock jitter (above 1 MHz) should be less than value specified by the A.C. Timing section.

14 Functional Timing

All functional timing diagrams assume that polarity control is not being applied to input and output data and clock lines (i.e. polarity control bits in the S/UNI-1x155 registers are set to their default states).

14.1 Transmit ATM UTOPIA Level 2 System Interface

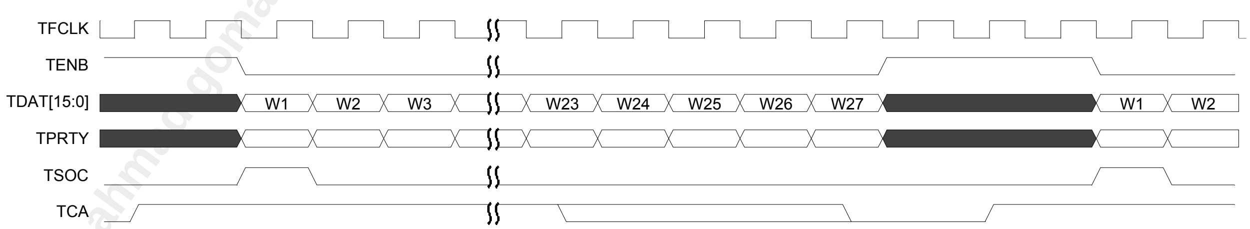
The ATM UTOPIA Level 2 System Interface is compatible with the UTOPIA Level 2 specification (see References). The S/UNI-1x155 only supports the 16-bit and 8–bit mode of operation.

The Transmit UTOPIA Level 2 System Interface Timing diagram presented in Figure 39 illustrates the operation of the system side transmit FIFO interface, in a single PHY configuration. Assertion of the transmit cell available output, TCA, indicates that there is space available in the transmit FIFO for at least one ATM cell structure. Deassertion of TCA occurs when the FIFO is filled with the number of ATM cells indicated by the register bits FIFODP[1:0]. TCA will only deassert one clock cycle after TSOC is sampled high and may assert at any time. If the TCA is configured to deassert early before the FIFO is truly full, the FIFO will accept additional cells even if TCA is inactive. At any time, if the upstream does not have a cell to write, it must deassert TENB.

As well, the TCA may be configured to deassert after the last word of a cell is written into the FIFO (FIFO is full) or as the cell is being written into the FIFO (FIFO is near full). In addition, the register bit TCAINV can be used to invert the polarity of TCA.

TSOC must be high during the first word of the ATM cell structure and must be present for the start of each cell. Thus, TSOC will mark the first word of the ATM cell. When TSOC is asserted and the previous byte transferred was not the end of an ATM cell structure, the system interface realigns itself to the new timing, and the previous partially transferred cell is dropped

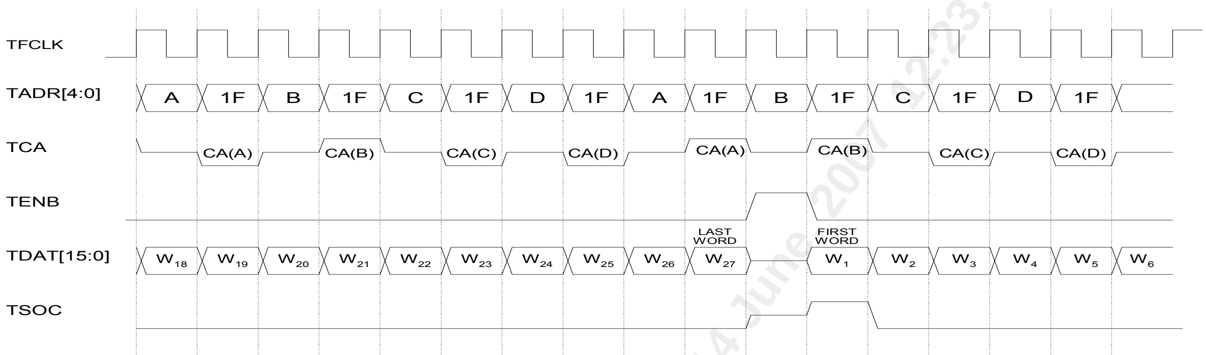
Figure 39 Transmit UTOPIA Level 2 System Interface Timing



The Transmit UTOPIA Level 2 System Interface Timing diagram (Figure 40) illustrates an example of the operation of the system side transmit FIFO interface, in a Multi-PHY configuration. The example shows four S/UNIs 1x155, A, B, C and D, which are polled until the end of a transmission cycle. TCA shows that A and B S/UNIs are ready to accept cells. S/UNI B is selected with the rising edge of TFCLK while TENB is high and the TADR[4:0] bus has the value "B". For a proper operation in a Multi-PHY mode the TSEN pin should be connected high.

Under some conditions, TCA has been observed to deassert for 1 to 3 clock cycles, immediately following the TSOC pulse. Please see Errata.

Figure 40 Transmit UTOPIA Level 2 System Interface Timing(MPHY)

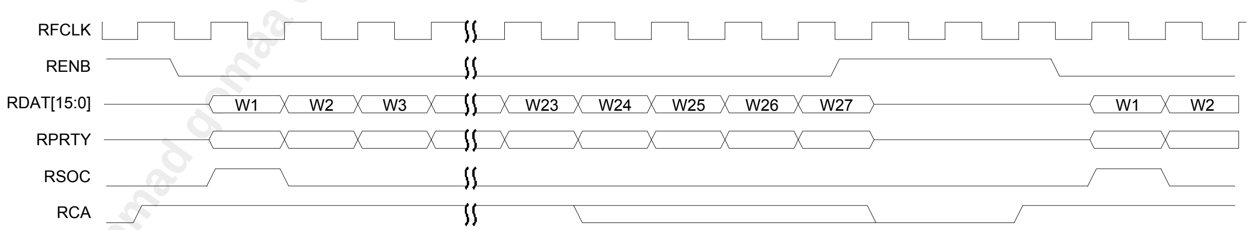


14.2 Receive ATM UTOPIA Level 2 System Interface

The Receive UTOPIA Level 2 System Interface Timing diagram (Figure 41) illustrates the operation of the system side receive interface. The RXCP indicates that a cell is available by asserting the receive cell available output RCA. RCA remains high until the receive FIFO is empty. After RCA is deasserted, it remains low for a minimum of one RFCLK clock cycle and can then reassert to indicate that there are additional cells available in the FIFO.

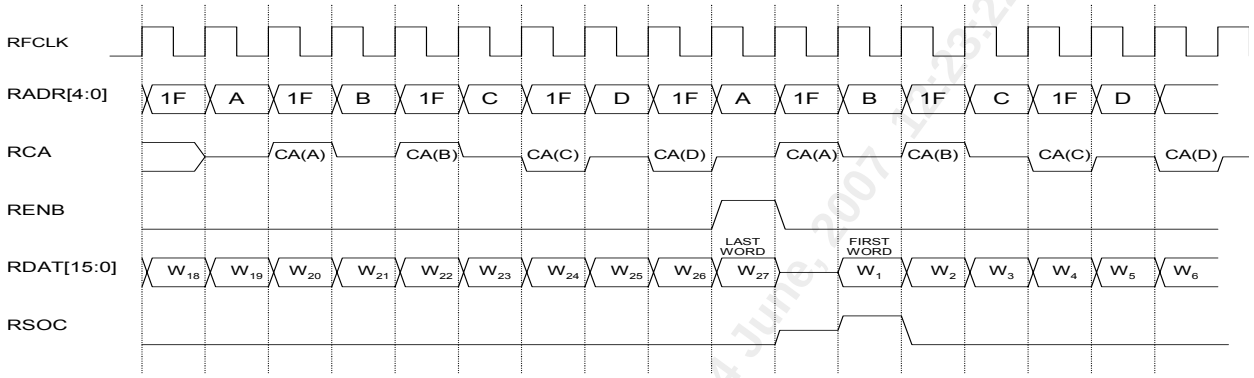
At any time, the downstream reader can throttle back the reception of words by deasserting RENB. The RDAT[15:0], RPRTY and RSOC signals tri-state when RENB is sampled deasserted. RSOC is high during the first word of the ATM cell structure and is present for the start of each cell. Thus, RSOC will mark the H1 to H4 bytes in the ATM cell structure.

Figure 41 Receive UTOPIA Level 2 System Interface Timing



The Receive UTOPIA Level 2 System Interface Timing diagram (Figure 42) illustrates an example of the operation of the system side receive FIFO interface, in a Multi-PHY configuration. The example shows four S/UNIs 1x155, A, B, C and D, which are polled until the end of a reception cycle. RCA shows that A and B S/UNIs are ready to accept cells. S/UNI A is selected with the rising edge of RFCLK while RENB is high and the RADR[4:0] bus has the value “A”. For a proper operation in a Multi-PHY mode the TSEN pin should be connected high.

Figure 42 Receive UTOPIA Level 2 System Interface Timing(MPHY)



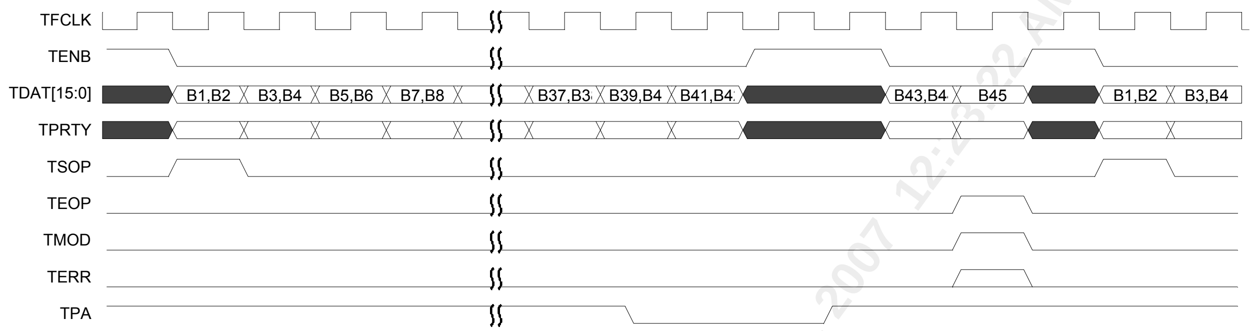
14.3 Transmit Packet over SONET/SDH (POS) Level 2 System Interface

The Packet over SONET/SDH (POS) Level 2 System Interface is compatible with the POS-PHY Level 2 specification (see References). The S/UNI-1x155 supports only the 16-bit mode of operation.

The Transmit POS Level 2 System Interface Timing diagram (Figure 43) illustrates the operation of the system side transmit FIFO interface, in a single PHY configuration. Assertion of the transmit packet available output, TPA, indicates that there is space available in the transmit FIFO. Deassertion of TPA occurs when the FIFO is filled to the depth indicated by the register TPAHWM[7:0]. The exact octet that triggers the deassertion of TPA depends on the particular timing relationship between the internal SONET/SDH clock and TFCLK, and for that reason is not precise. However the TXFP is always conservative. Thus, when TPA deasserts with no more than TPAHWM[7:0] bytes in the FIFO remains. If TPA is asserted and the upstream is ready to write a byte, the upstream device should assert TENB. At any time, if the upstream does not have a word to write, it must deassert TENB. In addition, the register bit TPAINV can be used to invert the meaning of TPA.

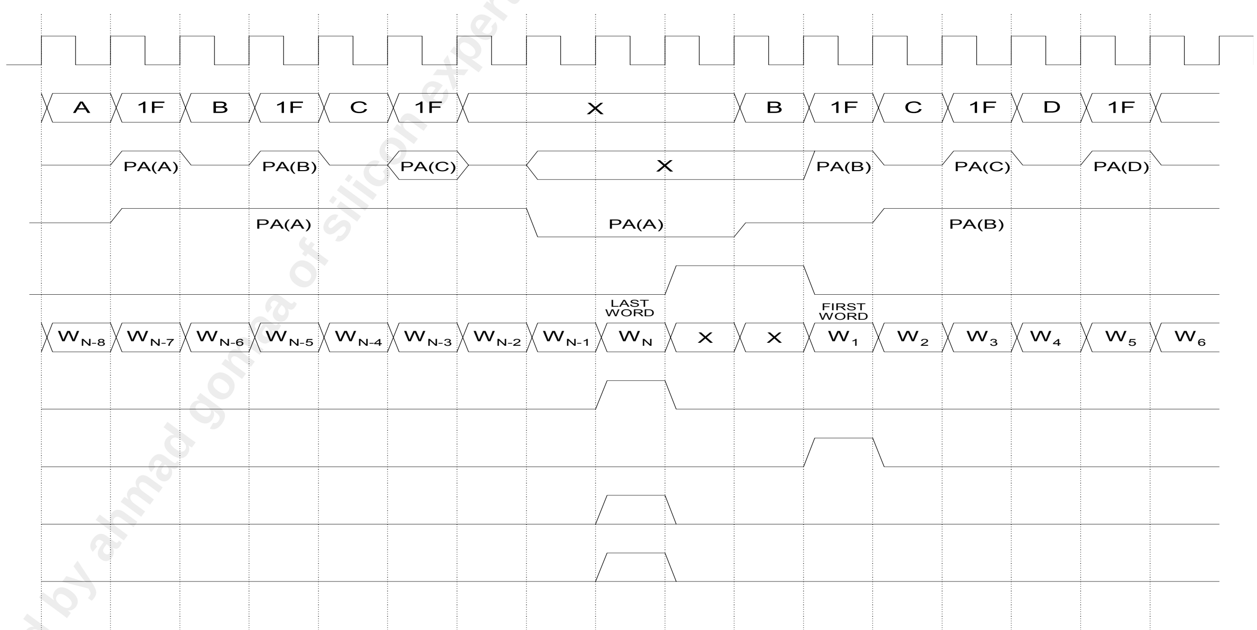
TSOP must be high during the first word of the packet and must be present for the start of each packet. TEOP must be high during the last packet word/byte transferred. During a packet transfer, every word must be composed of two bytes and TMOD shall be low. TMOD is used to during the last word of the packet transfer to determine if the word is composed of one or two bytes. It is legal to assert TSOP and TEOP at the same time. This case occurs when a 1-byte or a 2-byte packet is transferred. When TSOP is asserted and the previous word transfer was not marked with TEOP, the system interface realigns itself to the new timing, and the previous packet is aborted.

Figure 43 Transmit POS Level 2 System Interface Timing



The Transmit POS Level 2 System Interface Timing diagram (Figure 44) illustrates an example of the operation of the system side transmit FIFO interface, in a Multi- PHY configuration. The example shows four S/UNIs 1x155, A, B, C and D, which are polled until the end of a transmission cycle. PTPA and STPA show that S/UNI B is the only one ready to accept cells, while S/UNI C status is ignored. S/UNI B is selected with the rising edge of TFCLK while TENB is high and the TADR[4:0] bus has the value "B". In this example S/UNI A was configured to deassert STPA two words before the FIFO was empty. For a proper operation in a Multi-PHY mode the TSEN pin should be connected high.

Figure 44 Transmit POS Level 2 System Interface Timing(MPHY)



14.4 Receive Packet over SONET/SDH (POS) Level 2 System Interface

The Receive POS Level 2 System Interface Timing diagram (Figure 45) illustrates the operation of the interface, in a single PHY configuration.. The RXFP indicates that a packet is available by asserting the receive packet available output RPA. RPA remains high until the receive FIFO is empty. After RPA is deasserted, it remains low for a minimum of one RFCLK clock cycle and then can assert to indicate that there are additional packets available in the FIFO. At any time, the downstream reader can throttle back the reception of words by deasserting RENB.

RSOP is high during the first word of the packet. REOP is high during the last packet word. During a packet transfer every word is composed of two bytes. RMOD is used during the last word of the packet transfer to determine if the last word is composed of one or two bytes. It is legal to assert RSOP and REOP at the same time. This case occurs when a 1-byte or a 2-byte packet is transferred. Packets that were subject to an error (aborted, length violation, FIFO overrun, etc) will be marked by RERR high during the last word transfer.

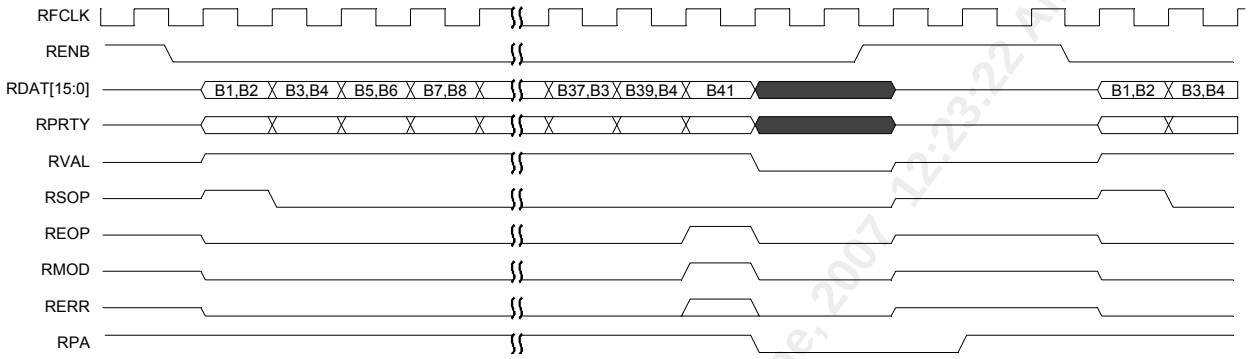
When a packet with less than 6 bytes arrives (from the line side), the receive packet available signal (RPA) may assert before data is available. In this condition, RPA will assert between 1 to 3 RFCLK clock cycles before the data is available and will remain asserted for 1 to 3 RFCLK clock cycles. When the Link Layer device attempts to read the packet by asserting read enable (RENB), it may find that there is no valid data available (receive data valid signal (RVAL) remains de-asserted). RPA will correctly assert again later when data is available. At this time the RVAL signal will be asserted indicating valid data.

With packets greater than 6 bytes, the RPA signal will assert, de-assert and then reassert 1 to 3 RFCLK cycles later (same as the above case with packets less than 6 bytes). However, if the Link layer device attempts to read the packet on the basis of the first occurrence of RPA, it will read valid data (RVAL will be asserted), even if RPA may be de-asserted.

This early assertion of RPA will not cause any data corruption if RVAL is used to qualify the data that is read. It is recommended that RVAL always be used to qualify receive data. The operation of RPA may cause a slight reduction bandwidth on receive side of the POS-PHY interface. However, since there is ample bandwidth on the POS-PHY interface there will be no impact on performance of functionality.

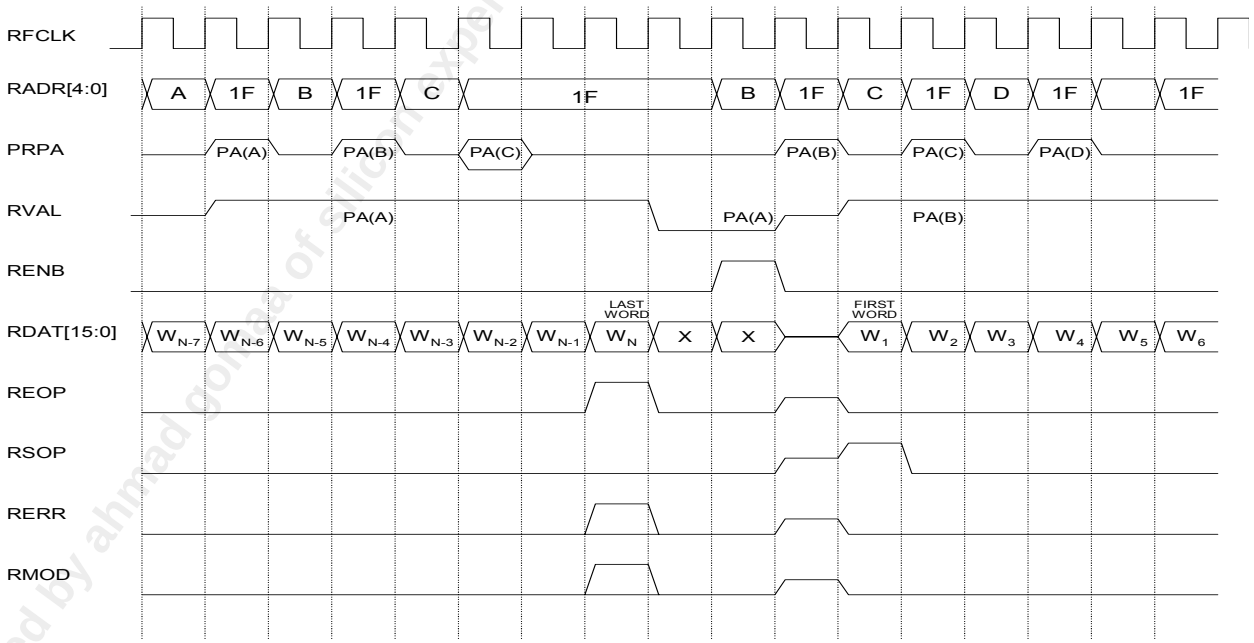
During the transfer of a packet, valid data is marked by RVAL high. If the FIFO under-runs, or if REOP is encountered, the RXFP will de-assert RVAL to halt the transfer, and the link layer device must deassert RENB. A new transfer may then be started by asserting RENB when RPA indicates that more packet data is available.

Figure 45 Receive POS Level 2 System Interface Timing



The Receive POS Level 2 System Interface Timing diagram (Figure 46) illustrates an example of the operation of the system side transmit FIFO interface, in a Multi- PHY configuration. The example shows four S/UNIs 1x155, A, B, C and D, which are polled until the end of a reception cycle. PTPA and STPA show that S/UNI B is the only one ready to accept cells, while S/UNI C status is ignored. S/UNI B is selected with the rising edge of RFCLK while RENB is high and the RADR[4:0] bus has the value "B". For a proper operation in a Multi-PHY mode the TSEN pin should be connected high. In this mode several PHY layer devices share the RDAT[15:0], RSOP, REOP, RMOD and RPRTY signals.

Figure 46 Receive POS Level 2 System Interface Timing(MPHY)



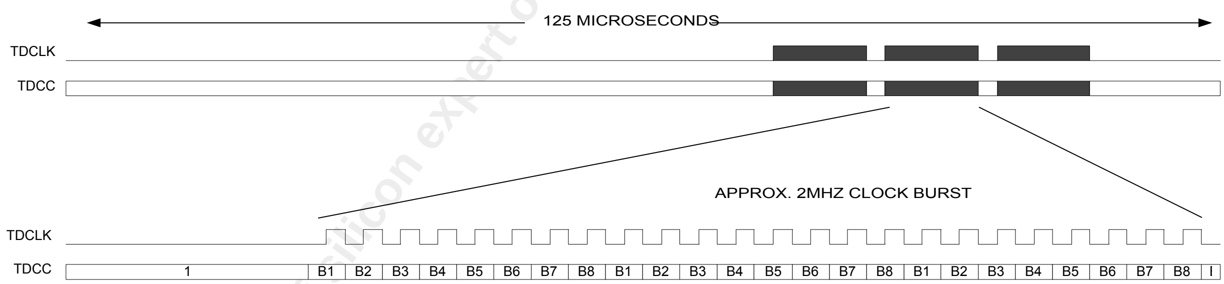
The receive POS-PHY Level 2 interface cannot support full bandwidth with arbitrarily small consecutive packets. In general, the minimum consecutive packet size the interface can transfer without overrunning the receive FIFO in the TXFP is a function of how quickly the downstream logic reselects the S/UNI-1x155 after an end of packet is transferred on the bus. If the number of cycles between packet transfers (that is, the number of RFCLK cycles between RVAL going low, RENB deasserting and then reasserting) is kept small, the minimum full-bandwidth packet size can be as low as 15 to 20 bytes.

14.5 Transmit Data Communication Channels

The SUNI-1x155 provides access to Line or Section Data Communications Channel (DCC). The TDCC with its clock TDCLK provides either the section or line DCC channel based on the DCCSEL register.

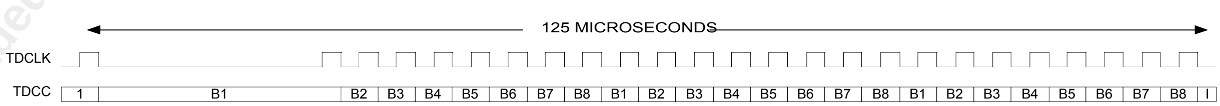
The Transmit Line Data Link Clock and Data Insertion diagram (Figure 47) shows the relationship between the TDCC serial data input, and its associated TDCLK. In this mode, TDCLK is a 2.16 MHz, 67%(high)/33%(low) duty cycle clock that is gapped to produce a 576 kHz nominal rate. TDCC is sampled on the rising edge of TDCLK. The D4-D12 bytes shifted in to the S/UNI-1x155 in the frame shown are inserted in the corresponding transport overhead channels in the next frame.

Figure 47 Transmit Line Data Link Clock and Data Insertion



The Transmit Section Data Link Clock and Data Insertion diagram (Figure 48) shows the relationship between the TDCC serial data input, and its associated TDCLK. In this mode, TDCLK is a 216 kHz, 50% duty cycle clock that is gapped to produce a 192 kHz nominal rate. TDCC is sampled on the rising edge of TDCLK. The D1-D3 bytes shifted in to the S/UNI-1x155 in the frame shown are inserted in the corresponding transport overhead channels in the next frame.

Figure 48 Transmit Section Data Link Clock and Data Insertion

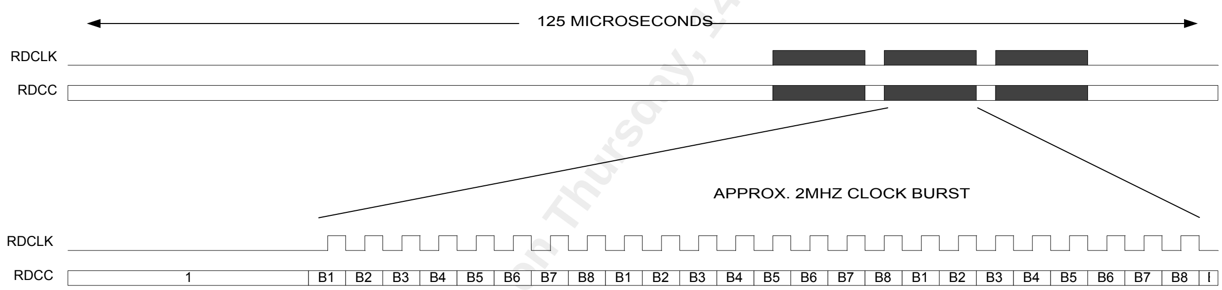


14.6 Receive Data Communication Channels

The SUNI-1x155 provides access to Line or Section Data Communications Channels (DCC). The RDCC with their clocks RDCLK provide either the section or line DCC channels based on the DCCSEL register.

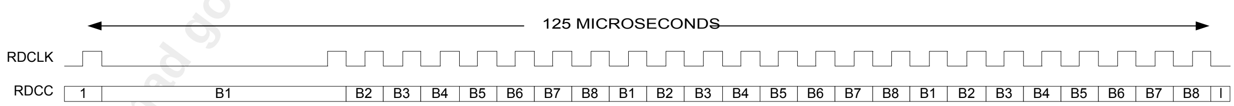
The Receive Line Data Link Clock and Data Extraction Timing diagram (Figure 49) shows the relationship between the RDCC serial data output and its associated RDCLK when configured for line DCC. In this mode, RDCLK is a 2.16 MHz, 67%(high)/33%(low) duty cycle clock that is gapped to produce a 576 kHz nominal rate. RDCC is updated on the falling edge of RDCLK. The D4-D12 bytes shifted out of the S/UNI-1x155 in the frame shown are extracted from the corresponding transport overhead channels in the previous frame.

Figure 49 Receive Line Data Link Clock and Data Extraction



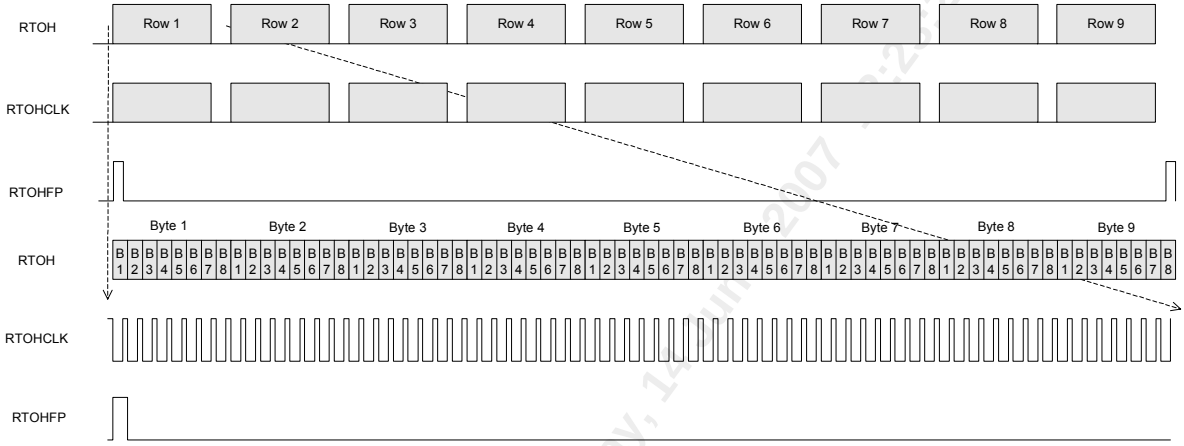
The Receive Section Data Link Clock and Data Extraction Timing diagram (Figure 50) shows the relationship between a RDCC serial data output and its associated RDCLK when configured for section DCC. In this mode, RDCLK is a 216 kHz, 50% duty cycle clock that is gapped to produce a 192 kHz nominal rate. RDCC is updated on the falling edge of RDCLK. The D1-D3 bytes shifted out of the S/UNI-1x155 in the frame shown are extracted from the corresponding transport overhead channels in the previous frame.

Figure 50 Receive Section Data Link Clock and Data Extraction



14.7 Transport Overhead Extraction and Insertion

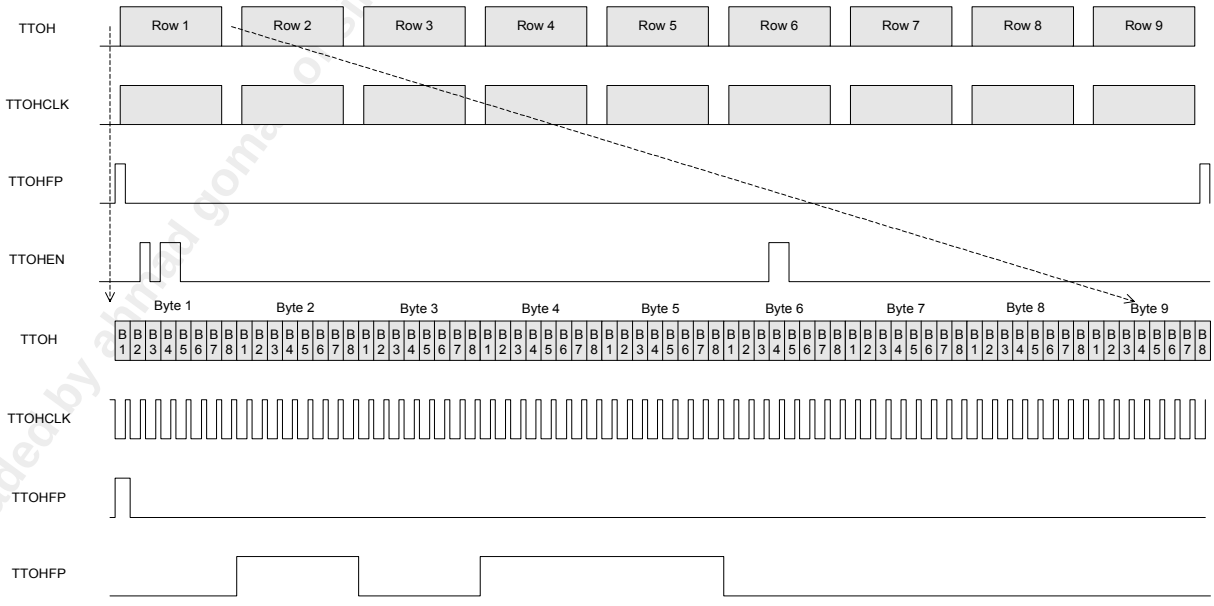
Figure 51 Transport Overhead Extraction



The transport overhead extraction timing diagram above illustrates the transport overhead extraction interface for STS-3c (STM-1). The transport overhead extraction clock, RTOHCLK is nominally a 5.184 MHz clock and is derived from the receive line clock, RCLK. The entire transport overhead (the complete 9 row by 9 column structure) is extracted for the STS-3c (STM-1) stream and is serialized on RTOH over a frame period (125 µs).

RTOHFP and RTOH are updated on the falling edge of RTOHCLK.

Figure 52 Transport Overhead Insertion



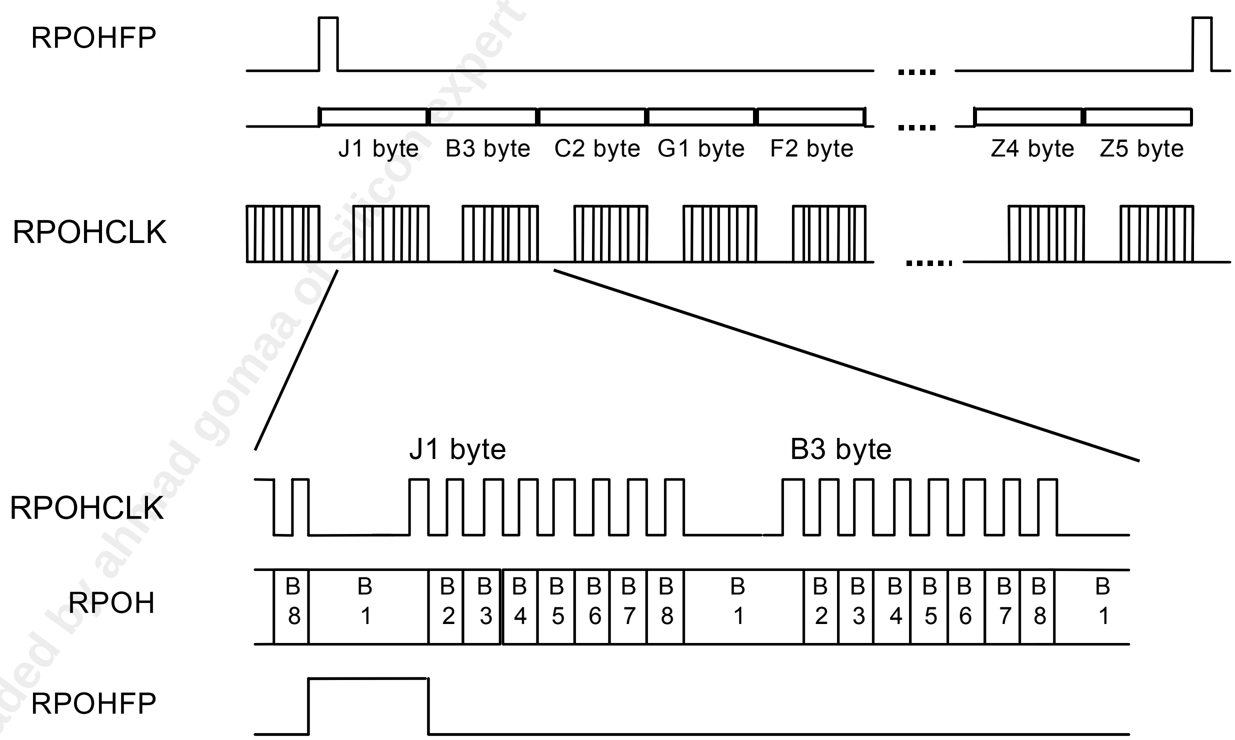
The transport overhead insertion timing diagram above illustrates the transport overhead insertion interface. Output TTOHCLK is nominally a 5.184 MHz clock and is used to update output TTOHFP, and to sample input TTOH and TTOHEN. The value sampled on TTOHEN during the first overhead bit position of a given overhead byte determines whether the byte sampled on TTOH is inserted in the STS-3c (STM-1) stream. TTOHEN is held high during the bit 1 position of the Byte 2 (here, third A1), Byte 4 (first A2) and B4 (second A2) in the TTOH stream. The eight bit values sampled on input TTOH during the third A1 byte period , first A2 byte period and second A2 byte period are inserted in the corresponding byte positions in the STS-3c stream. Similarly, TTOHEN is held low during the bit 1 position of the others bytes of Row 1. The default values are inserted in the corresponding byte positions in the STS-3c (STM-1) stream ignoring the contents of TTOH.

An error insertion feature is also provided for the B1. When TTOH is held high during any of the bit positions corresponding to these bytes, the corresponding bit is inverted before being inserted in the STS-3c (STM-1) stream (TTOHEN must be sampled high during the first bit position to enable the error insertion mask).

TTOH and TTOHEN are sampled on the rising edge of TTOHCLK. TTOHFP is updated on the falling edge of TTOHCLK.

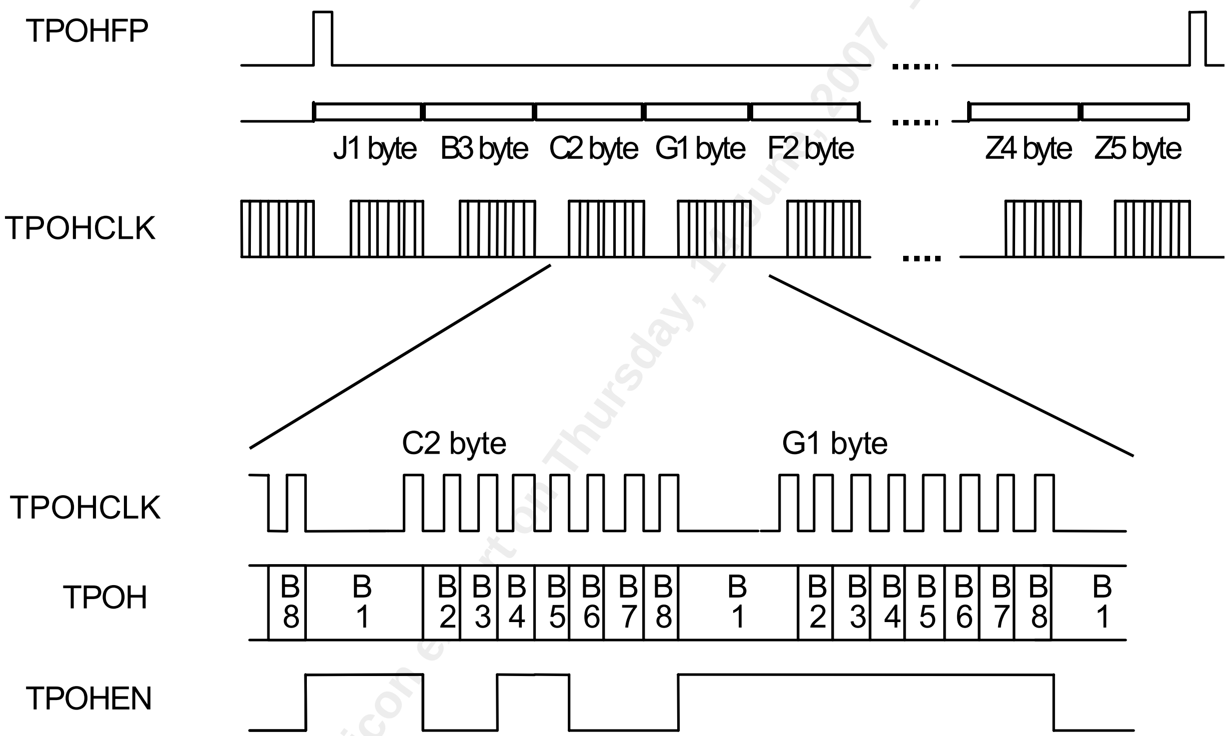
14.8 Path Overhead Extraction and Insertion

Figure 53 Receive Path Overhead Extraction Timing



The figure above shows the receive path overhead extraction to a low speed serial stream. RPOHCLK are nominally 576 KHz clocks. The entire path overhead (J1, B3, C2, G1, F2, H4, Z3, Z4, Z5 bytes) is extracted, serialized and placed on RPOH over a frame period. For each byte, the most significant bit is transmitted first. RPOHFP mark the most significant bit of the J1 byte.

Figure 54 Transmit Path Overhead Insertion Timing



The figure above shows the transmit path overhead insertion from a low speed serial stream. TPOHCLK are nominally 576 KHz clocks. The entire path overhead, except B3 and H4, (J1, C2, G1, F2, Z3, Z4, Z5 bytes) can be inserted into the transmit stream via TPOH over a frame period. In each byte, the most significant bit is transmitted first. TPOHFP mark the most significant bit of the J1 byte. TPOHEN control the insertion of data on TPOH on a byte basis. The data on TPOH is inserted in the path overhead of the transmit stream if TPOHEN is set high at the first bit position of the byte to be inserted. TPOHEN is set high during bits 1, 4 and 5 of the C2 byte and the entire G1 byte. For this sample configuration, the G1 byte and the C2 byte will be taken from TPOH.

An error insertion feature is provided for the B3 or H4 byte. When TPOHEN and TPOH are both set high, the corresponding path BIP bit or tributary multiframe sequence bit will be inverted before insertion in the transmit stream.

15 Absolute Maximum Ratings

Maximum rating are the worst case limits that the device can withstand without sustaining permanent damage. They are not indicative of normal mode operation conditions.

Table 21 Absolute Maximum Ratings

Storage Temperature	-40°C to +125°C
VDDO Supply Voltage	-0.3V to +4.6V
VDDQ Supply Voltage	-0.3V to +4.6V
VDDI Supply Voltage	-0.3V to +3.5V
Voltage on Any Pin	-0.3V to +5.5V
Static Discharge Voltage	±1000 V
Latch-Up Current per Pin	±100 mA
DC Input Current	±20 mA
Lead Temperature	+230°C
Absolute Maximum Junction Temperature	+150°C

16 D.C. Characteristics

T_A = -40°C to T_J =+125°C, V_{DDI} = 2.5V ± 5%, V_{DDO} = 3.3V ± 8%, V_{AVD} = 3.3V ± 5%,
(Typical Conditions: T_A = 25°C, V_{DDI} = 2.5V, V_{DDO} = 3.3V, V_{AVD} = 3.3V)

Table 22 D.C Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{VDDI}	Power Supply	2.37	2.5	2.63	Volts	
V_{DDO}	Power Supply	3.04	3.3	3.56	Volts	
V_{DDQ}	Power Supply	3.04	3.3	3.56	Volts	
V_{AVD}	Power Supply	3.14	3.3	3.47	Volts	
V_{IL}	Input Low Voltage	0		0.8	Volts	Guaranteed Input Low voltage.
V_{IH}	Input High Voltage	2.0			Volts	Guaranteed Input High voltage.
V_{OL}	Output or Bi-directional Low Voltage		0.2	0.4	Volts	Guaranteed output low voltage at VDDO=2.97V and I_{OL}=maximum rated for pad.
V_{OH}	Output or Bi-directional High Voltage	2.4	2.6		Volts	Guaranteed output high voltage at VDDO=2.97V and I_{OH}=maximum rated current for pad.
V_{T+}	Reset Input High Voltage	2.0			Volts	Applies to RSTB and TRSTB only.
V_{T-}	Reset Input Low Voltage			0.8	Volts	Applies to RSTB and TRSTB only.
V_{TH}	Reset Input Hysteresis Voltage		0.3		Volts	Applies to RSTB and TRSTB only.
V_{PECLI+}	Input PECL High Voltage	V_{PECL} - 1.165	V_{PECL} - 0.955	V_{PECL} -0.880	Volts	V_{PECL} = 5.0V or 3.3V
V_{PECLI-}	Input PECL Low Voltage	V_{PECL} - 1.810	V_{PECL} - 1.700	V_{PECL} - 1.470	Volts	V_{PECL} = 5.0V or 3.3V
V_{PECLIC}	Input PECL Common Mode Voltage	V_{PECL} - 1.490	V_{PECL} - 1.329	V_{PECL} - 1.180	Volts	V_{PECL} = 5.0V or 3.3V
V_{PECLO+}	Output PECL High Voltage	V_{PECL} -0.880	V_{PECL} - 0.955	V_{PECL} - 1.025	Volts	V_{PECL} = 5.0V or 3.3V (APSO outputs only).
V_{PCLO5-}	Output PECL Low Voltage	V_{PECL} - 1.620	V_{PECL} - 1.705	V_{PECL} - 1.810	Volts	V_{PECL} = 5.0V or 3.3V (APSO outputs only).
I_{ILPU}	Input Low Current	-100	-50	-4	µA	V_{IL} = GND. Notes 1 and 3.
I_{IHPU}	Input High Current	-10	0	+10	µA	V_{IH} = V_{DDO}. Notes 1 and 3.
I_{IL}	Input Low Current	-10	0	+10	µA	V_{IL} = GND. Notes 2 and 3.
I_{IH}	Input High Current	-10	0	+10	µA	V_{IH} = V_{DDO}. Notes 2 and 3.
C_{IN}	Input Capacitance		5		pF	t_A=25°C, f = 1 MHz

Symbol	Parameter	Min	Typ	Max	Units	Conditions
C_{OUT}	Output Capacitance		5		pF	t_A=25°C, f = 1 MHz
C_{IO}	Bi-directional Capacitance		5		pF	t_A=25°C, f = 1 MHz

Notes on D.C. Characteristics:

1. Input pin or bi-directional pin with internal pull-up resistor.
2. Input pin or bi-directional pin without internal pull-up resistor.
3. Negative currents flow into the device (sinking); positive currents flow out of the device (sourcing).

17 Power Information

Table 23 Power Requirements

Conditions	Parameter	Typ[1,3]	High[4]	Max[2]	Units
ATM Mode APS Enabled	IDDOP(2.5 V)	0.088		0.100	A
	IDDOP(3.3 V Dig)	0.066		0.119	A
	IDDOP(3.3 V Anlg)	0.016		0.036	A
	Total Power	0.491	0.654	-	W
POS Mode APS Enabled	IDDOP (2.5 V)	0.104		0.118	A
	IDDOP (3.3 V)	0.058		0.112	A
	IDDOP(3.3 V Anlg)	0.016		0.036	A
	Total Power	0.504	0.670	-	W
ATM Mode APS Disabled	IDDOP (2.5 V)	0.088		0.100	A
	IDDOP (3.3 V)	0.049		0.091	A
	IDDOP(3.3 V Anlg)	0.016		0.036	A
	Total Power	0.435	0.576	-	W
POS Mode APS Disabled	IDDOP (2.5 V)	0.085		0.097	A
	IDDOP (3.3 V)	0.053		0.098	A
	IDDOP(3.3 V Anlg)	0.016		0.036	A
	Total Power	0.440	0.586		W

Notes:

1. Typical IDD values are calculated as the mean value of current under the following conditions: typically processed silicon, nominal supply voltage, T_J=60 °C, outputs loaded with 30 pF (if not otherwise specified), and a normal amount of traffic or signal activity. These values are suitable for evaluating typical device performance in a system
2. Max IDD values are currents guaranteed by the production test program and/or characterization over process for operating currents at the maximum operating voltage and operating temperature that yields the highest current (including outputs loaded to 30 pF, unless otherwise specified)
3. Typical power values are calculated using the formula:

   Power = ∑i(VDDNomi x IDDTypi)

   Where i denotes all the various power supplies on the device, VDDNomi is the nominal voltage for supply i, and IDDTypi is the typical current for supply i (as defined in note 1 above). These values are suitable for evaluating typical device performance in a system
4. High power values are a “normal high power” estimate and are calculated using the formula:

   Power = ∑i(VDDMaxi x IDDHighi)

   Where i denotes all the various power supplies on the device, VDDMaxi is the maximum operating voltage for supply i, and IDDHighi is the current for supply i. IDDHigh values are calculated as the mean value plus two sigmas (2σ) of measured current under the following conditions: T_J=105° C, outputs loaded with 30 pF (if not otherwise specified). These values are suitable for evaluating board and device thermal characteristics.

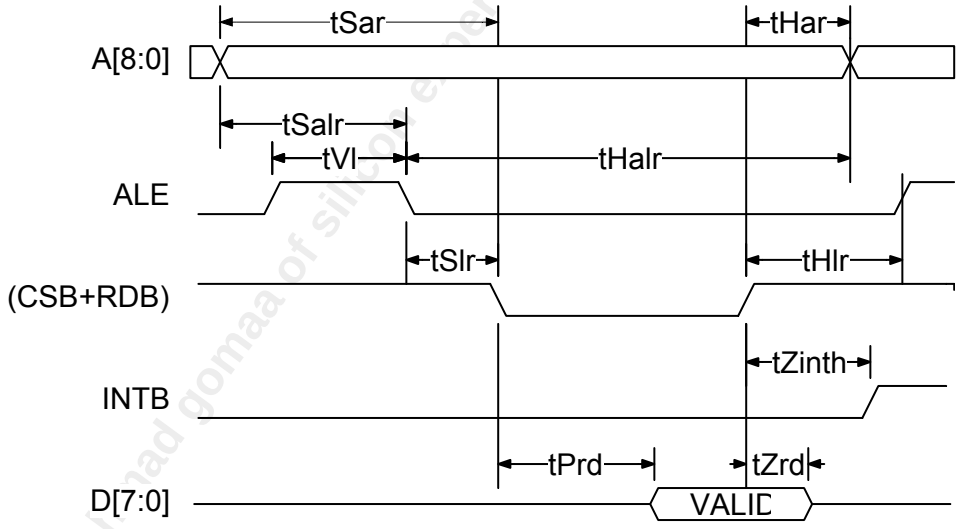
18 Microprocessor Interface Timing Characteristics

T_A = -40°C to T_J =+125°C, V_{DDI} = 2.5V ± 5%, V_{DDO} = 3.3V ± 8%, V_{AVD} = 3.3V ± 5%,

Table 24 Microprocessor Interface Read Access (Figure 55)

Symbol	Parameter	Min	Max	Units
tSAR	Address to Valid Read Set-up Time	10	—	ns
tHAR	Address to Valid Read Hold Time	5	—	ns
tSALR	Address to Latch Set-up Time	10	—	ns
tHALR	Address to Latch Hold Time	10	—	ns
tVL	Valid Latch Pulse Width	5	—	ns
tSLR	Latch to Read Set-up	0	—	ns
tHLR	Latch to Read Hold	5	—	ns
tPRD	Valid Read to Valid Data Propagation Delay	—	70	ns
tZRD	Valid Read Negated to Output Tri-state	—	20	ns
tZINTH	Valid Read Negated to Output Tri-state	—	50	ns

Figure 55 Microprocessor Interface Read Timing



Notes on Microprocessor Interface Read Timing:

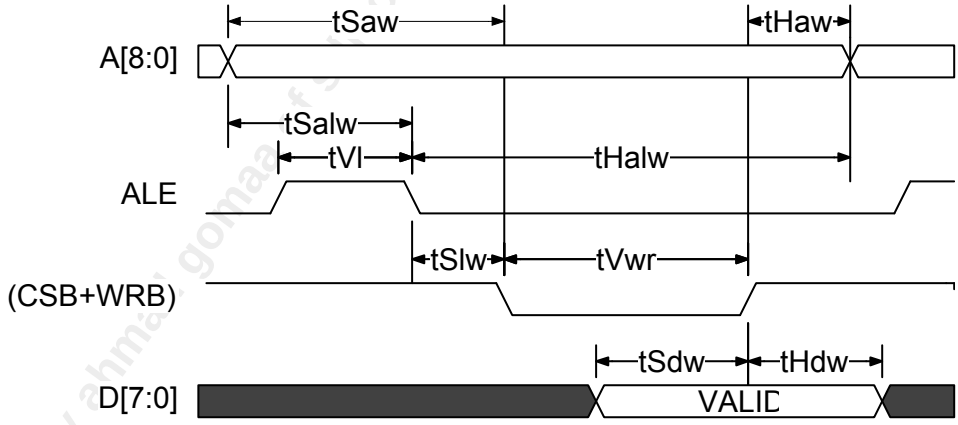
1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[7:0]).
3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.

4. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tS_{ALR}, tH_{ALR}, tV_L, tS_{LR}, and tH_{LR} are not applicable.
5. Parameter tH_{AR} is not applicable if address latching is used.
6. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
7. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
8. Output tri-state delay is the time in nanoseconds from the 1.4 Volt of the reference signal to the point where the total current delivered through the output is less than or equal to the leakage current.

Table 25 Microprocessor Interface Write Access (Figure 56)

Symbol	Parameter	Min	Max	Units
tSAW	Address to Valid Write Set-up Time	10	—	ns
tSDW	Data to Valid Write Set-up Time	20	—	ns
tSALW	Address to Latch Set-up Time	10	—	ns
tHALW	Address to Latch Hold Time	10	—	ns
tVL	Valid Latch Pulse Width	5	—	ns
tSLW	Latch to Write Set-up	0	—	ns
tHLW	Latch to Write Hold	5	—	ns
tHDW	Data to Valid Write Hold Time	5	—	ns
tHAW	Address to Valid Write Hold Time	5	—	ns
tVWR	Valid Write Pulse Width	40	—	ns

Figure 56 Microprocessor Interface Write Timing



Notes on Microprocessor Interface Write Timing:

1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals.
2. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tS_{ALW}, tH_{ALW}, tV_L, tS_{LW}, and tH_{LW} are not applicable.
3. Parameter tH_{AW} is not applicable if address latching is used.

4. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
5. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

19 A.C. Timing Characteristics

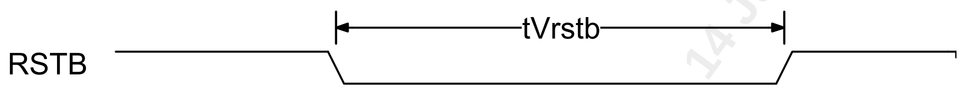
T_A= -40°C to T_J +125°C, V_{DDI} = 2.5V ± 5%, V_{DDO} = 3.3V ± 8%, V_{AVD} = 3.3V ± 5%,

19.1 System Reset Timing

Table 26 RSTB Timing (Figure 57)

Symbol	Description	Min	Max	Units
tVRSTB	RSTB Pulse Width	100	—	ns

Figure 57 RSTB Timing Diagram



19.2 OC-3 Interface Timing Characteristics

Table 27 OC-3 Interface Timing

Symbol	Description	Min	Typical	Max	Units
F_{REFCLK}	Required frequency for REFCLK_P and REFCLK_N inputs (Bellcore spec for +/-20ppm clock sources); all conditions		19.44		MHz
$T_{REF, RISE}$	Rise time for REFCLK+ and REFCLK- inputs; all conditions	-	-	1	ns
$T_{REF, FALL}$	Fall time for REFCLK+ and REFCLK- inputs; all conditions	-	-	1	ns
DC_{REF}	Duty Cycle for REFCLK+ and REFCLK- inputs; all conditions	45	50	55	%
$T_{REF, JITTER}$	Jitter acceptable on REFCLK+ and REFCLK- inputs (between 12 kHz and 1.3 MHz) all conditions[1] With extrnal APS enabled.	-	-	30	ps (rms)
r_B	Bit rate for OC-3 compatible transmit and receive data	-	155.52 = 8 x F_{refclk}	-	Mb/s

Note:

1. 30ps rms (Max) values has been mathematically derived from statistical results and board-level assumptions.

19.3 UTOPIA Level 2 System Interface Timing

Table 28 Transmit UTOPIA Level 2 System Interface Timing (Figure 58)

Symbol	Description	Min	Max	Units
fTFCLK	TFCLK Frequency	25	52	MHz
DTFCLK	TFCLK Duty Cycle	40	60	%
JTFCLK	TFCLK Peak to Peak Jitter (> 1 MHz)		1	ns
tS_{TENB}	TENB Set-up time to TFCLK	4		ns
tH_{TENB}	TENB Hold time to TFCLK	1		ns
tS_{TDAT}	TDAT[15:0] Set-up time to TFCLK	4		ns
tH_{TDAT}	TDAT[15:0] Hold time to TFCLK	1		ns
tS_{TPRTY}	TPRTY Set-up time to TFCLK	4		ns
tH_{TPRTY}	TPRTY Hold time to TFCLK	1		ns
tS_{TSOC}	TSOC Set-up time to TFCLK	4		ns
tH_{TSOC}	TSOC Hold time to TFCLK	1		ns
tS_{TADR}	TADR[4:0] Set-up time to TFCLK	4		ns
tH_{TADR}	TADR[4:0] Hold time to TFCLK	1		ns
tP_{TCA}	TFCLK High to TCA Valid	1	10	ns
tZ_{TCA}	TFCLK High to TCA Tri-State	1	12	ns
tZB_{TCA}	TFCLK High to TCA Driven	1	12	ns

Figure 58 Transmit UTOPIA Level 2 System Interface Timing Diagram

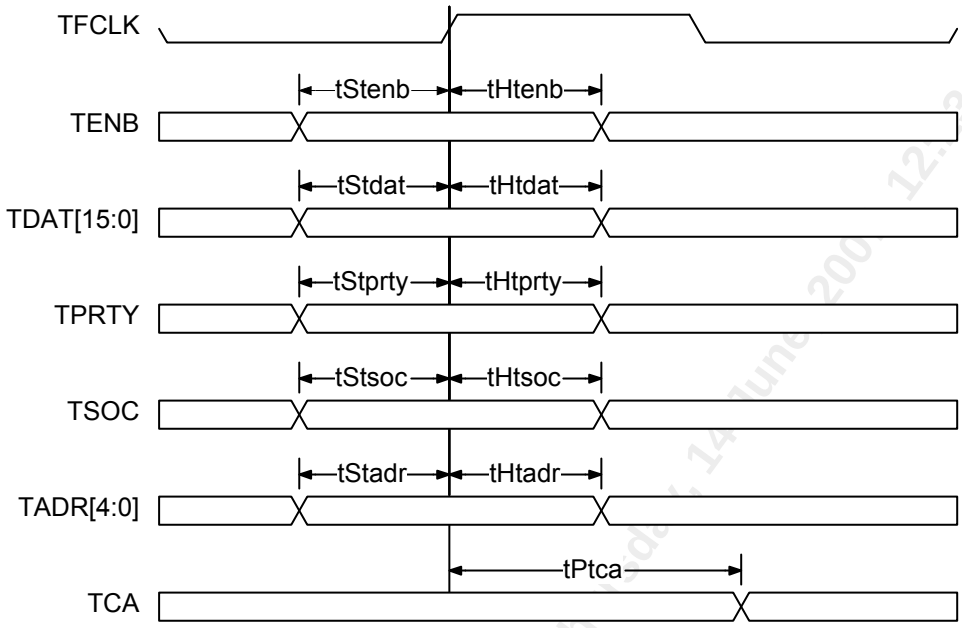
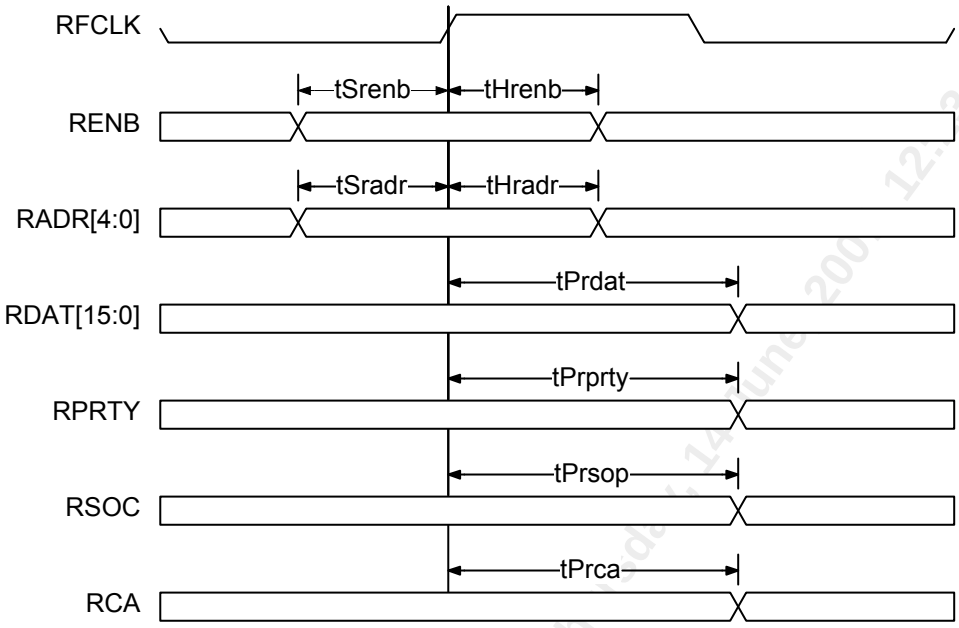


Table 29 Receive UTOPIA Level 2 System Interface Timing (Figure 59)

Symbol	Description	Min	Max	Units
f_{RFCLK}	RFCLK Frequency	25	52	MHz
D_{RFCLK}	RFCLK Duty Cycle	40	60	%
J_{RFCLK}	RFCLK Peak to Peak Jitter (> 1 MHz)		1	ns
tS_{RENB}	RENB Set-up time to RFCLK	4		ns
tH_{RADR}	RADR[4:0] Hold time to RFCLK	1		ns
tS_{RADR}	RADR[4:0] Set-up time to RFCLK	4		ns
tH_{RENB}	RENB Hold time to RFCLK	1		ns
tP_{RDAT}	RFCLK High to RDAT[15:0] Valid	1	10	ns
tZ_{RDAT}	RFCLK High to RDAT[15:0] Tri-State	1	12	ns
tZB_{RDAT}	RFCLK High to RDAT[15:0] Driven	1	12	ns
tP_{RSOC}	RFCLK High to RSOC Valid	1	10	ns
tZ_{RSOC}	RFCLK High to RSOC Tri-State	1	12	ns
tZB_{RSOC}	RFCLK High to RSOC Driven	1	12	ns
tP_{RPRTY}	RFCLK High to RPRTY Valid	1	10	ns
tZ_{RPRTY}	RFCLK High to RPRTY Tri-State	1	12	ns
tZB_{RPRTY}	RFCLK High to RPRTY Driven	1	12	ns
tP_{RCA}	RFCLK High to RCA Valid	1	10	ns
tZ_{RCA}	RFCLK High to RCA Tri-State	1	12	ns
tZB_{RCA}	RFCLK High to RCA Driven	1	12	ns

Figure 59 Receive UTOPIA Level 2 System Interface Timing Diagram



19.4 POS Level 2 System Interface Timing

Table 30 Transmit POS-PHY Level 2 System Interface Timing (Figure 60)

Symbol	Description	Min	Max	Units
f_{TFCLK}	TFCLK Frequency	25	52	MHz
D_{TFCLK}	TFCLK Duty Cycle	40	60	%
J_{TFCLK}	TFCLK Peak to Peak Jitter (> 1 MHz)		1	ns
t_{STENB}	TENB Set-up time to TFCLK	4		ns
t_{HTENB}	TENB Hold time to TFCLK	0		ns
t_{STDAT}	TDAT[15:0] Set-up time to TFCLK	4		ns
t_{HTDAT}	TDAT[15:0] Hold time to TFCLK	0		ns
t_{STMOD}	TMOD Set-up time to TFCLK	4		ns
t_{HTMOD}	TMOD Hold time to TFCLK	0		ns
t_{STPRTY}	TPRTY Set-up time to TFCLK	4		ns
t_{HTPRTY}	TPRTY Hold time to TFCLK	0		ns
t_{STSOP}	TSOP Set-up time to TFCLK	4		ns
t_{HTSOP}	TSOP Hold time to TFCLK	0		ns
t_{STEOP}	TEOP Set-up time to TFCLK	4		ns
t_{HTEOP}	TEOP Hold time to TFCLK	0		ns
t_{STERR}	TERR Set-up time to TFCLK	4		ns
t_{HTERR}	TERR Hold time to TFCLK	0		ns
t_{STADR}	TADR[4:0] Set-up time to TFCLK	4		ns
t_{HTADR}	TADR[4:0] Hold time to TFCLK	0		ns
t_{PTPA}	TFCLK High to TPA Valid	1	10	ns
t_{ZSTPA}	TFCLK High to STPA Tri-State	1	12	ns
t_{ZBSTPA}	TFCLK High to STPA Driven	1	12	ns

Figure 60 Transmit POS-PHY Level 2 System Interface Timing

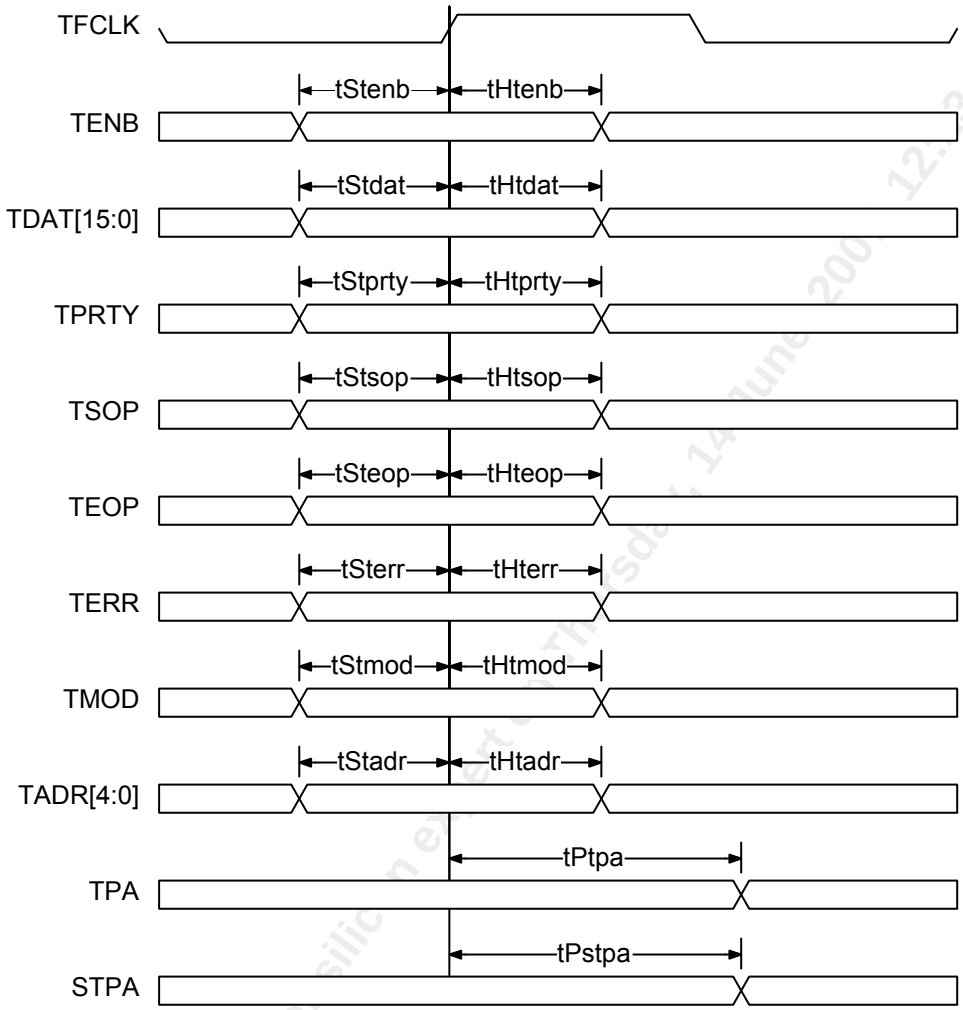
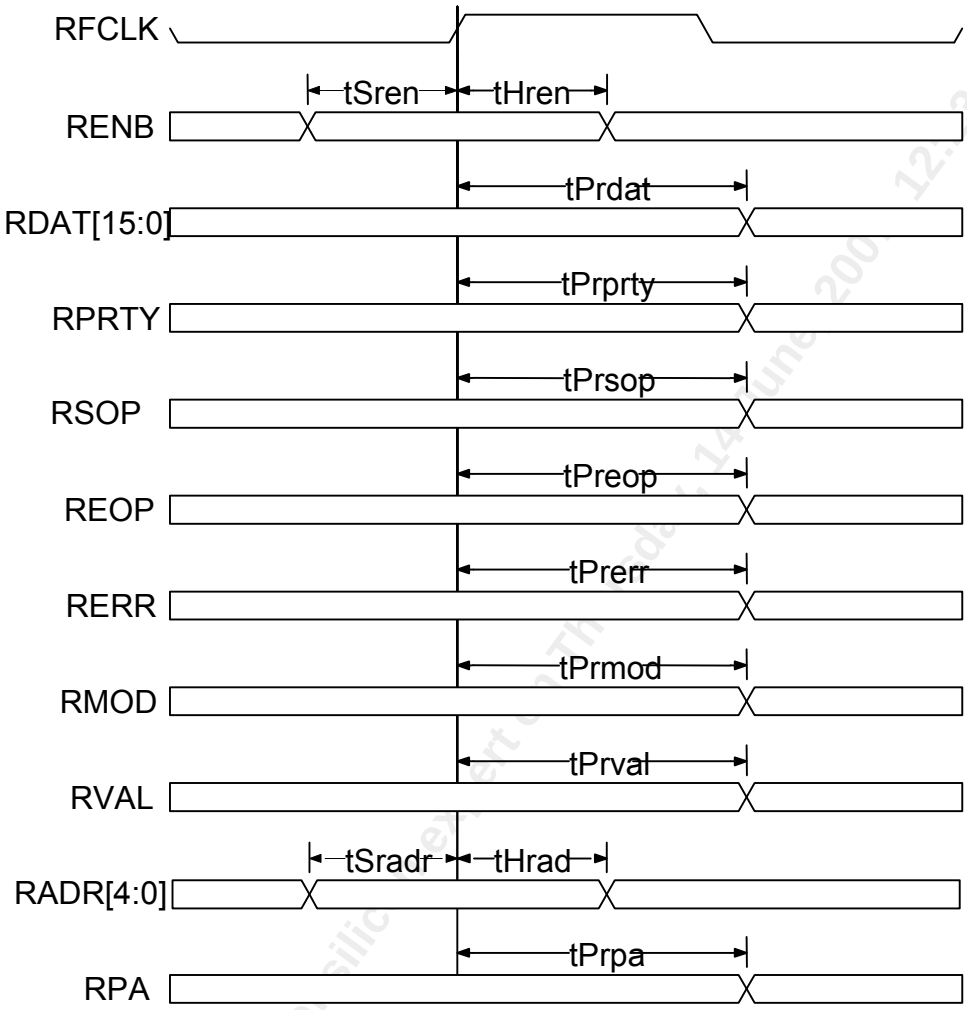


Table 31 Receive POS-PHY Level 2 System Interface Timing (Figure 61)

Symbol	Description	Min	Max	Units
f_{RFCLK}	RFCLK Frequency	25	52	MHz
D_{RFCLK}	RFCLK Duty Cycle	40	60	%
J_{RFCLK}	RFCLK Peak to Peak Jitter (> 1 MHz)		1	ns
tS_{RENB}	RENB Set-up time to RFCLK	4		ns
tH_{RENB}	RENB Hold time to RFCLK	0		ns
tS_{RADR}	RADR[4:0] Set-up time to RFCLK	4		ns
tH_{RADR}	RADR[4:0] Hold time to RFCLK	0		ns
tP_{RDAT}	RFCLK High to RDAT[15:0] Valid	1	10	ns
tZ_{RDAT}	RFCLK High to RDAT[15:0] Tri-State	1	12	ns
tZB_{RDAT}	RFCLK High to RDAT[15:0] Driven	1	12	ns
tP_{RPRTY}	RFCLK High to RPRTY Valid	1	10	ns
tZ_{RPRTY}	RFCLK High to RPRTY Tri-State	1	12	ns
tZB_{RPRTY}	RFCLK High to RPRTY Driven	1	12	ns
tP_{RSOP}	RFCLK High to RSOP Valid	1	10	ns
tZ_{RSOP}	RFCLK High to RSOP Tri-State	1	12	ns
tZB_{RSOP}	RFCLK High to RSOP Driven	1	12	ns
tP_{REOP}	RFCLK High to REOP Valid	1	10	ns
tZ_{REOP}	RFCLK High to REOP Tri-State	1	12	ns
tZB_{REOP}	RFCLK High to REOP Driven	1	12	ns
tP_{RERR}	RFCLK High to RERR Valid	1	10	ns
tZ_{RERR}	RFCLK High to RERR Tri-State	1	12	ns
tZB_{RERR}	RFCLK High to RERR Driven	1	12	ns
tP_{RVAL}	RFCLK High to RVAL Valid	1	10	ns
tZ_{RVAL}	RFCLK High to RVAL Tri-State	1	12	ns
tZB_{RVAL}	RFCLK High to RVAL Driven	1	12	ns
tP_{RPA}	RFCLK High to RPA Valid	1	10	ns
tZ_{RPA}	RFCLK High to RPA Tri-State	1	12	ns
tZB_{RPA}	RFCLK High to RPA Driven	1	12	ns
tP_{RMOD}	RFCLK High to RMOD Valid	1	10	ns
tZ_{RMOD}	RFCLK High to RMOD Tri-State	1	12	ns
tZB_{RMOD}	RFCLK High to RMOD Driven	1	12	ns

Figure 61 Receive POS-PHY Level 2 System Interface Timing

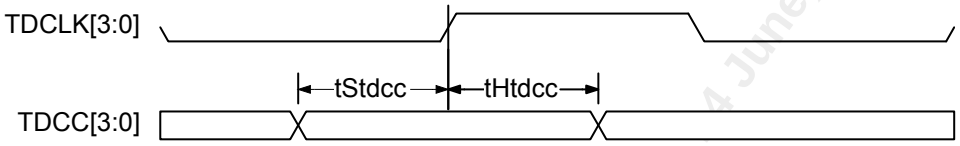


19.5 Transmit DCC Interface Timing

Table 32 Transmit DCC Interface Timing (Figure 62)

Symbol	Description	Min	Max	Units
tS_{TDCC}	TDCC Set-up time to TDCLK	25		ns
tH_{TDCC}	TDCC Hold time to TDCLK	25		ns

Figure 62 Transmit DCC Interface Timing

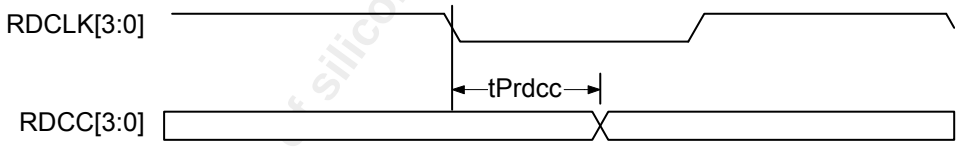


19.6 Receive DCC Interface Timing

Table 33 Receive DCC Interface Timing (Figure 63)

Symbol	Description	Min	Max	Units
tP_{RDCC}	RDCLK low to RDCC Valid	-20	20	ns

Figure 63 Receive DCC Interface Timing

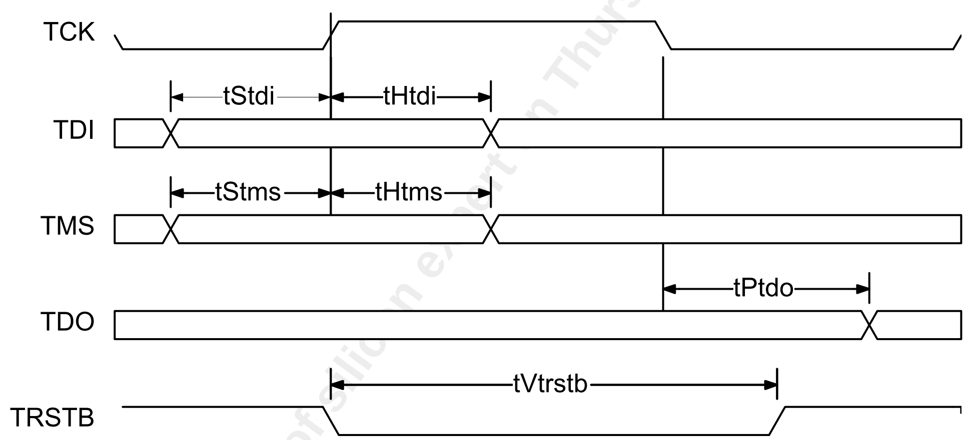


19.7 JTAG Test Port Timing

Table 34 JTAG Port Interface (Figure 64)

Symbol	Description	Min	Max	Units
	TCK Frequency		4	MHz
	TCK Duty Cycle	40	60	%
tS_{TMS}	TMS Set-up time to TCK	25		ns
tH_{TMS}	TMS Hold time to TCK	25		ns
tS_{TDI}	TDI Set-up time to TCK	25		ns
tH_{TDI}	TDI Hold time to TCK	25		ns
tP_{TDO}	TCK Low to TDO Valid	2	50	ns
tV_{TRSTB}	TRSTB Pulse Width	100		ns

Figure 64 JTAG Port Interface Timing



Notes on Input Timing

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Notes on Output Timing

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Output propagation delays are measured with a 50 pF load on the outputs.
3. Output tri-state delay is the time in nanoseconds from the 1.4 Volt of the reference signal to the point where the total current delivered through the output is less than or equal to the leakage current.

20 Thermal Information

This product is designed to operate over a wide temperature range and is suited for outside plant equipment[1].

Table 35 Outside Plant Thermal Information

Maximum long-term operating junction temperature (T_J) to ensure adequate long-term life.	[105] °C
Maximum junction temperature (T_J) for short-term excursions with guaranteed continued functional performance[2]. This condition will typically be reached when the local ambient temperature reaches 85 °C.	[125] °C
Minimum ambient temperature (T_A)	[-40] °C

Table 36 Thermal Resistance vs. Air Flow[3]

Airflow	Natural Convection	200 LFM	400 LFM
θ_{JA} (°C/W)	[38.8]	[33.3]	[31.3]

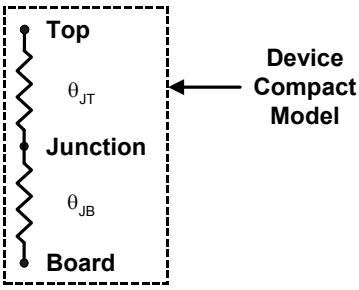


Table 37 Device Compact Model[4]

Junction-to-Top Thermal Resistance, θ_{JT}	[12] °C/W
Junction-to-Board Thermal Resistance, θ_{JB}	[27.7] °C/W

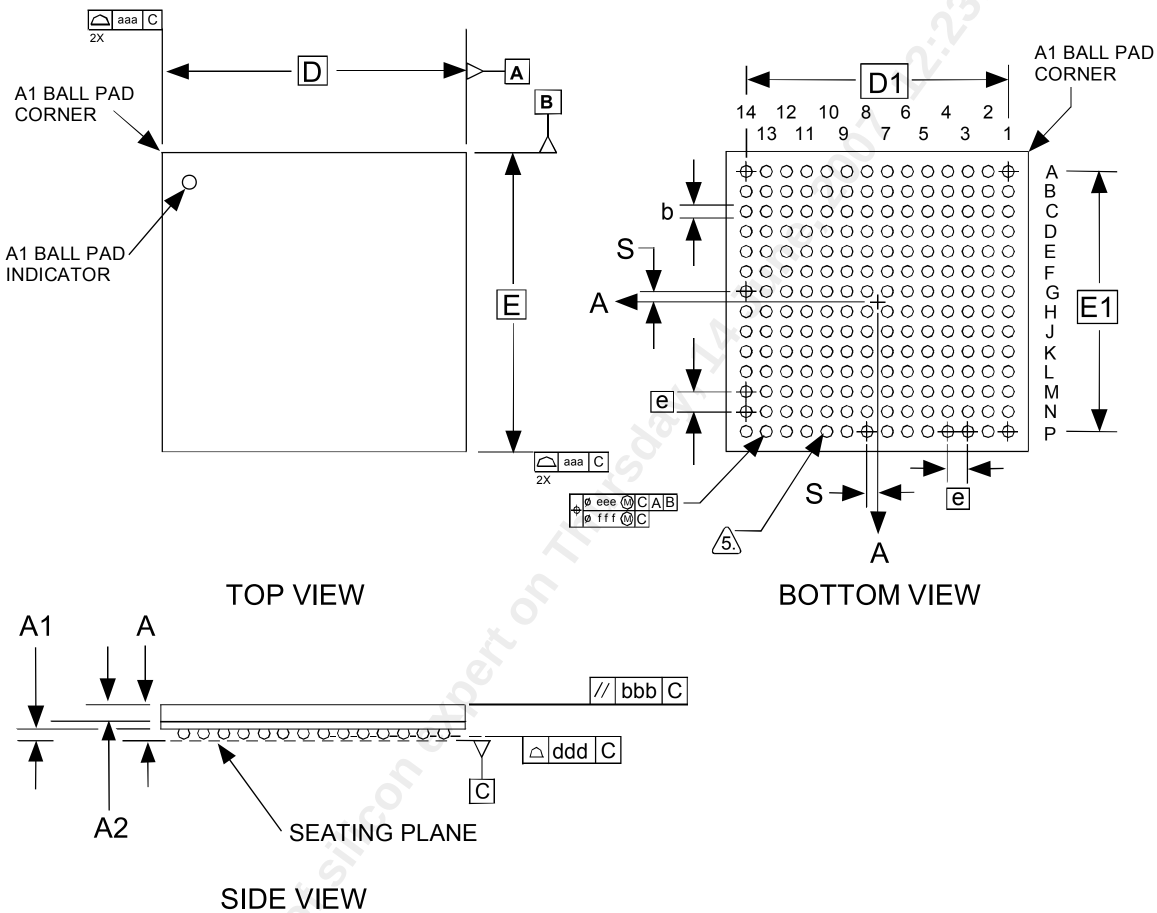
Power depends upon the operating mode. To obtain power information, refer to 'High' power values in section 17.

Notes

1. The minimum ambient temperature requirement for Outside Plant Equipment meets the minimum ambient temperature requirement for Industrial Equipment
2. Short-term is used as defined in Telcordia Technologies Generic Requirements GR-63-Core Core; for more information about this standard, see section 4.
3. θ_{JC}, the junction-to-case thermal resistance, is a measured nominal value plus two sigma. θ_{JB}, the junction-to-board thermal resistance, is obtained by simulating conditions described in JEDEC Standard JESD 51-8; for more information about this standard, see section 4.
4. θ_{SA} is the thermal resistance of the heat sink to ambient. θ_{CS} is the thermal resistance of the heat sink attached material. The maximum θ_{SA} required for the airspeed at the location of the device in the system with all components in place

21 Mechanical Information

Figure 65 Mechanical Drawing 196-pin stPBGA



NOTES: 1) ALL DIMENSIONS IN MILLIMETER.
2) DIMENSION aaa DENOTES PACKAGE BODY PROFILE.
3) DIMENSION bbb DENOTES PARALLEL.
4) DIMENSION ddd DENOTES COPLANARITY.
5) DIAMETER OF SOLDER MASK OPENING IS 0.400 ± 0.025 MM (SMD).

PACKAGE TYPE: 196 SMALL THIN PLASTIC BALL GRID ARRAY - stPBGA															
BODY SIZE: 15 x 15 x 1.60 MM															
Dim.	A	A_1	A_2	D	D_1	E	E_1	b	e	aaa	bbb	ddd	eee	f f f	S
Min.	1.20	0.30	0.90	-	-	-	-	0.45	-	-	-	-	-	-	-
Nom.	1.40	0.40	1.00	15.00 BSC	13.00 BSC	15.00 BSC	13.00 BSC	0.50	1.00 BSC	-	-	-	-	-	0.50
Max.	1.60	0.50	1.10	-	-	-	-	0.55	-	0.20	0.35	0.20	0.30	0.10	-

Notes